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Graphene-based lateral heterostructure transistors exhibit better intrinsic performance than graphene-based vertical transistors as post-CMOS devices

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We investigate the intrinsic performance of vertical and lateral graphene-based heterostructure field-effect transistors, currently considered the most promising options to exploit graphene properties in post-CMOS electronics. We focus on three recently proposed graphene-based transistors, that in experiments have exhibited large current modulation. Our analysis is based on device simulations including the self-consistent solution of the electrostatic and transport equations within the Non-Equilibrium Green's Function formalism. We show that the lateral heterostructure transistor has the potential to outperform CMOS technology and to meet the requirements of the International Technology Roadmap for Semiconductors for the next generation of semiconductor integrated circuits. On the other hand, we find that vertical heterostructure transistors miss these performance targets by several orders of magnitude, both in terms of switching frequency and delay time, due to large intrinsic capacitances, and unavoidable current/capacitance tradeoffs.

Native graphene has a zero energy gap[1] and it is therefore not suitable as a channel material for digital electronics. In time, several options have been considered for opening a band gap in graphene, including imposing a lateral quantum confinement by cutting graphene flakes in narrow nanoribbons[2–4], chemical functionalization[5,6], and patterning hydrogen adsorpion[7,8], holes[9–11] or strain[12] in the graphene sheet. The option of using bilayer graphene, in which a gap can be electrostatically induced, has been also investigated[13,14].

These techniques are not sufficient: some of them are intrinsically unreliable (such as lateral confinement[4]), other introduce a gap of just few tens of meV, which is not sufficient for field effect transistor (FET) operation. All of them are likely to entail a degradation of graphene mobility[15,16]. Recently, advances based on materials engineering have demonstrated graphene-based "materials on demand", with tailored properties[17]. In particular, including graphene in heterostructures has been proved to offer many opportunities for the exploitation of its unique properties in devices that are both robust in terms of the operation principle and that can be completely switched off, as required in digital electronics. Different solutions have been proposed in the literature, including vertical or lateral heterostructures.

Yang *et al.*[18] have proposed and fabricated the "barristor", a vertical transport transistor based on a graphene/silicon heterojunction. The device structure is sketched in Figure 1 (a): the graphene layer acts as the source, whereas the bottom contact of the n-doped silicon region acts as the drain. Current flows from graphene to silicon by overcoming the Schottky barrier at the interface. Thanks to the graphene low density of states, which prevents complete screening of the electric field, a top gate separated from graphene by a dielectric layer can be used to modulate the effective height of the barrier, and thus the current.

A different vertical device has been proposed and fabricated by Britnell *et al.*[19] They considered an insulating layer of hexagonal boron nitride (hBN) stacked between two graphene layers, which act as the source and drain regions (Figure 1 (b)). Current is modulated by varying the voltage applied to an external gate, resulting in a modification of both the graphene density of states and the effective height of the barrier. As in the case of the barristor, also the operation of this device relies on the limited capability of graphene to screen the applied electric field. In the following we will call this device VHFET (Vertical Heterostructure FET).

A vertical graphene-based hot electron transistor has been proposed in Ref. 20 and demonstrated in Ref. 21. A graphene sheet, separated from the emitter and the collector regions by properly engineered insulating layers,

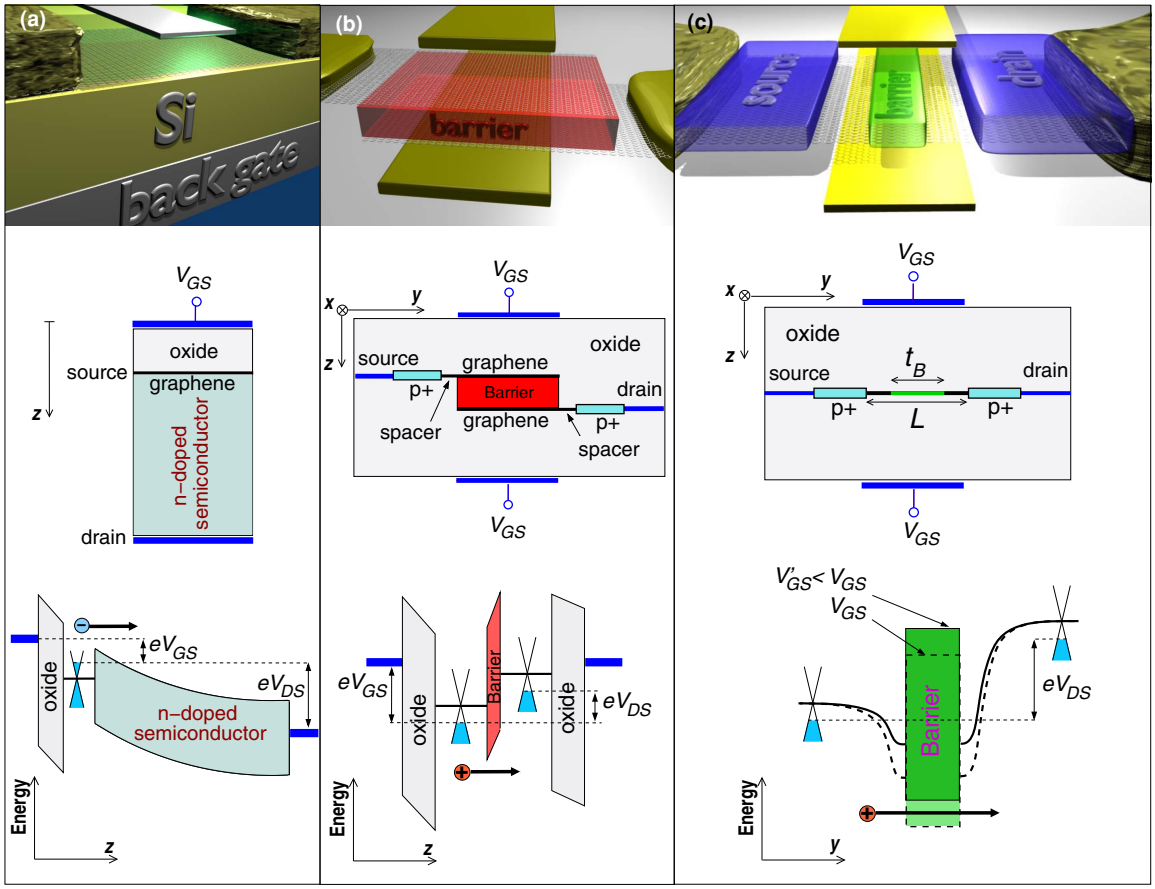

Figure 1 | Perspective view, cross-section of the simulation geometry and schematic band diagram of the considered devices: (a) barristor, (b) VHFET, (c) LHFET.

plays the role of the base electrode. In this case the extreme graphene thinness is used to obtain an ultra short "base" region, that would allow obtaining high transition frequencies.

A Graphene Lateral Heterostructure FET (LHFET) has been proposed by some of us[22,23] and has been recently demonstrated in experiments[24]. The channel consists of a graphene/insulator/graphene lateral heterostructure, where graphene regions act as the source and the drain, and the insulator, filling the central region of the channel (Figure 1 (c)), ensures current blocking at turn off. In light of the recent progress in the growth of seamless lateral graphene heterostructures[26–28], lattice-matched hBN and hexagonal boron carbon nitride (hBCN) have been proposed as insulator material[22,23].

The available simulation and experimental data[18–21,24,29,30] show that these devices exceed by far the performance of planar FETs with all-graphene channel and could reliably be used as switches in digital electronics. However, in order to assess whether they are really promising for transistor applications, their potential performance has to be compared with the current state of the art of CMOS technology and with the expectations for the next technology nodes, appearing in the most recent International Technology Roadmap for Semiconductors (ITRS).

In this paper we present a comparative analysis of three of the four above-mentioned devices, based on the evaluation of their performance potential. We will focus on field-effect devices, thus excluding at the moment the hot electron transistor, which would require more detailed understanding of partially ballistic vertical transport through the graphene layer[25].

We consider the main figures of merit for static and dynamic FET performance, using as a benchmark the ITRS for High Performance Logic. We assume a power supply voltage $V_{DD} = 0.6$ V, in order to be close to the ITRS requirements for the technology node corresponding to a 10 nm gate length.

Concerning the static figures of merit, we compute the I_{on}/I_{off} ratio, where I_{off} denotes the drain-to-source current I_{DS} in the OFF state ($V_{GS} = V_{GS}^{off}$; $|V_{DS}| = V_{DD}$) and I_{on} is the current in the ON state ($V_{GS} = V_{GS}^{off} + V_{DD}$; $|V_{DS}| = V_{DD}$); V_{GS}^{off} indicates the gate-source voltage (V_{GS}) in the off state, while V_{DS} indicate the drain-source voltage. We assume that in final device integration gate workfunction is adjusted as to have $V_{GS}^{off} = 0$ V for n-type FETs ($V_{GS}^{off} = V_{DD}$ for p-type FETs). For the LHFET we assume $I_{off} = 100$ nA/μm, as prescribed by the ITRS for High-Performance technology; for the barristor and the VHFET we have an additional degree of freedom (the length of the source) and we assume as I_{off} the value that maximizes the I_{on}/I_{off} ratio. For the sake of completeness, we also consider the minimum value of the subthreshold swing, SS_{min}, obtained from the transfer characteristic for $|V_{DS}| = V_{DD}$.

We quantify the switching speed by evaluating the intrinsic delay time τ[31]:

$$\tau = \frac{Q_{on} - Q_{off}}{I_{on}}, \tag{1}$$

where Q_{on} and Q_{off} indicate the mobile charge Q in the whole device in the ON and in the OFF state, respectively. Concerning energy consumption, we refer to the power-delay product PDP, defined as

$$PDP = V_{DD} I_{on} \tau = V_{DD}(Q_{on} - Q_{off}), \tag{2}$$

which represents the energy required to switch the device. Finally, we evaluate the high-frequency analog performance by computing the intrinsic cutoff frequency f_T of the device in the ON state. We adopt a

quasi-static model, assuming

$$f_T = \frac{1}{2\pi}\frac{\partial I_{DS}/\partial V_{GS}}{\partial Q/\partial V_{GS}}. \quad (3)$$

We do not consider the maximum oscillation frequency (the so-called f_{max}), although it is a more significant predictor of high-frequency performance than f_T, since it also depends on other parameters, like the contact resistance, that would include additional degrees of freedom and options beyond the scope of the present paper.

For each device we have considered the sensitivity to the most relevant tunable parameters, in order to perform a preliminary optimization, gain physical insights on the impact of various parameters and on possible performance limitations. As detailed in the Methods section, simulations have been performed with the NanoTCAD ViDES package[16,32]. Since we assume defectless devices, neglect gate leakage currents and any dissipative process (we assume that energy dissipation occurs only in the contacts), our results have to be considered an upper bound of the achievable performance. In the following we will show that, within the considered approximations, the LHFET is the only device that has the potential to exhibit better performance than that expected by the ITRS. The vertical heterostructure devices exhibit much worse performance, missing the ITRS benchmark of delay time by several orders of magnitude.

Results

In this section we discuss in detail the simulation results obtained for the three considered devices. The cross–section of the simulation geometries and a sketch of the band diagram for the devices are shown in Figure 1.

Barristor. In Figure 2 (a) we show the transfer characteristics obtained for a barristor based on a graphene/n-Si heterojunction, for a donor density $N_D = 10^{16}$ cm^{-3} and different values of the equivalent oxide thickness (EOT). As expected, the transfer characteristics become steeper as the EOT is reduced, due to the improvement in the electrostatic control of the Schottky barrier. Transfer characteristics roughly intersect at their inflection point, for $V_{GS} = -0.6$ V, where the Dirac point and the Fermi level coincide in graphene. As can be noticed, the current becomes almost constant for $V_{GS} < -1$ V, where it is dominated by the hole component injected by the drain, almost independent of V_{GS}. A suppression of I_{off}, and therefore an improvement of the I_{on}/I_{off} ratio, can be achieved by inhibiting the hole current, either increasing the doping or replacing silicon with a higher-bandgap material. To this purpose, we have considered gallium arsenide, which has a work function very close to that of silicon, and larger bandgap (~1.42 eV).

In Figure 2 (b) we compare the transfer characteristics obtained for different doping levels and different semiconductor layers (Si and GaAs), assuming EOT = 0.6 nm. The vertical shift of the transfer characteristics as doping increases is a consequence of the thinning of the almost triangular Schottky barrier, which enhances tunneling. We obtain the smallest value for the subthreshold swing, $SS_{min} \simeq 73$ mV/dec, in the case of the graphene/GaAs heterojunction with $N_D = 10^{18}$ cm^{-3}.

In Figure 3 (a) and (b) we report the values of the other figures of merit extracted in the considered cases. The PDP depends only weakly on doping and materials, taking a value of the order of ~10 fJ/μm^2. Results indicate that ($Q_{on} - Q_{off}$) is mainly determined by the mobile charge variation in graphene, essentially independent of the choice of semiconductor material and doping. Both τ and f_T improve as I_{on} increases, i.e. for larger semiconductor gap and high enough doping.

VHFET. We start by considering a pFET based on a graphene/hBN/graphene heterostructure with three hBN layers ($N_L = 3$). We adopt the double-gate architecture proposed in Ref. 30 (Figure 1 (b)), setting the EOT to 0.6 nm, and the tight-binding model described therein. In Figure 4 (a) we show the transfer characteristics for a VHFET with (triangles up) and without (circles) undoped spacers between the heavily doped source and

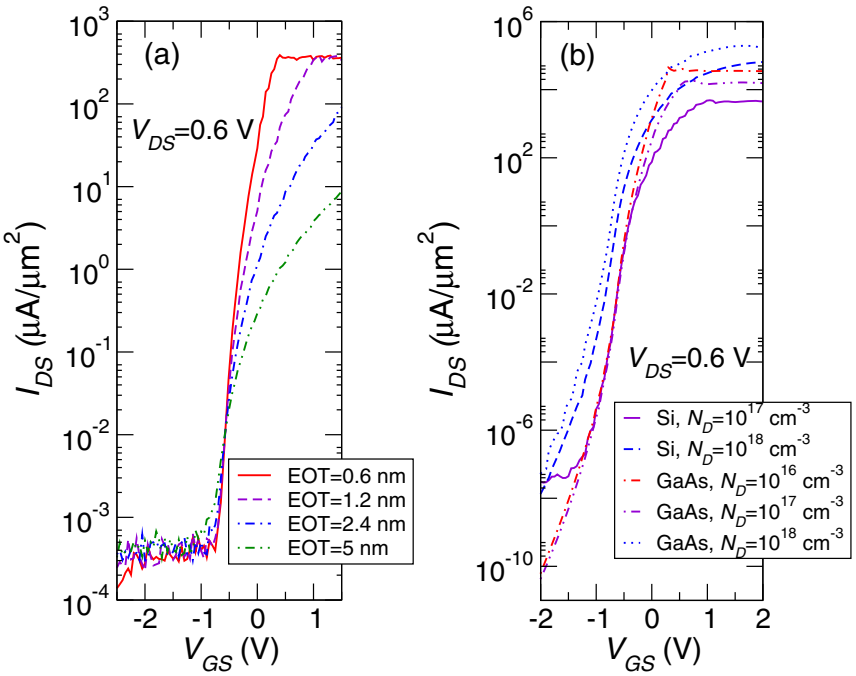

Figure 2 | (a) Simulation results for the barristor transfer characteristics for different values of EOT and $N_D = 10^{16}$ cm^{-3}. (b) Transfer characteristics obtained by considering graphene/Si and graphene/GaAs heterojunctions for EOT = 0.6 nm and different values of N_D.

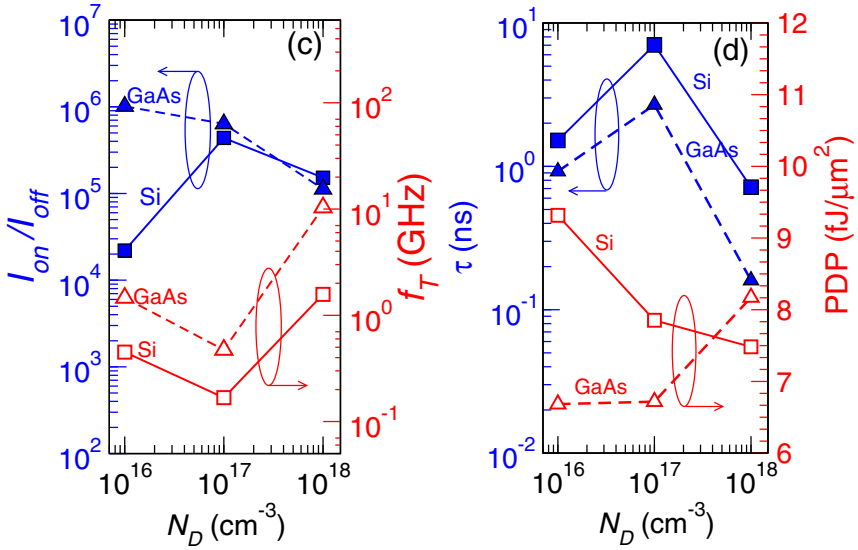

Figure 3 | **Static and dynamic figures of merit for the simulated barristors, for EOT = 0.6 nm and different values of N_D.**

drain regions and the graphene/hBN/graphene heterostructure. The quantity E_V indicated in the figure represents the energy difference between the insulator valence band and the Dirac point in graphene. The width of the spacers is 2 nm: we have verified that wider spacers do not improve results. The inclusion of spacers improves the I_{on}/I_{off} ratio by approximately one order of magnitude (Figure 5). We ascribe it to an increase in the capacitive coupling between the gates and the hBN, as a result of a suppression of the screening by the drain and source regions.

It is possible to further improve VHFET performance by replacing hBN with a material having a different electron affinity and/or a different bandgap. In this way it is indeed possible to obtain a shift of the subthreshold region of the device over a V_{GS} range in which the Dirac point in the top and bottom graphene channel is closer to the local Fermi level: this entails a reduction of the density of states in graphene and, thus, of the screening of the field induced by the gates. Candidate materials are hBCN compounds, which mantain hexagonal lattice structure and whose electronic properties can be tuned by varying the concentration of carbon atoms[28]. Due to the lack of a systematic characterization of these materials in the literature, we have defined an *ad hoc* tight-binding Hamiltonian, considering as a tunable parameter the energy difference E_V.

We obtain a general improvement of static and dynamic performance by considering $E_V = -0.5$ eV (Figure 5), due to the above-mentioned reduction in the graphene density of states and to a larger I_{on}. However, we observe only a small enhancement of the I_{on}/I_{off} ratio and of the subthreshold swing, SS_{min} (from ~330 mV/dec to ~315 mV/dec). The choice of different values of E_V can not improve significantly these results. In Figure 4 and Figure 5 we can also see that increasing the thickness of the dielectric to 5 atomic layers does not improve overall device performance. The I_{on}/I_{off} ratio increases, due to the higher slope of the transfer characteristic in the range $0.5\ \text{V} \lesssim V_{GS} \lesssim 1.5\ \text{V}$, where the electrostatic control over the barrier is more effective (*cf.* the Discussion section below), but τ and f_T fall by several orders of magnitude, due to the degradation of I_{on}.

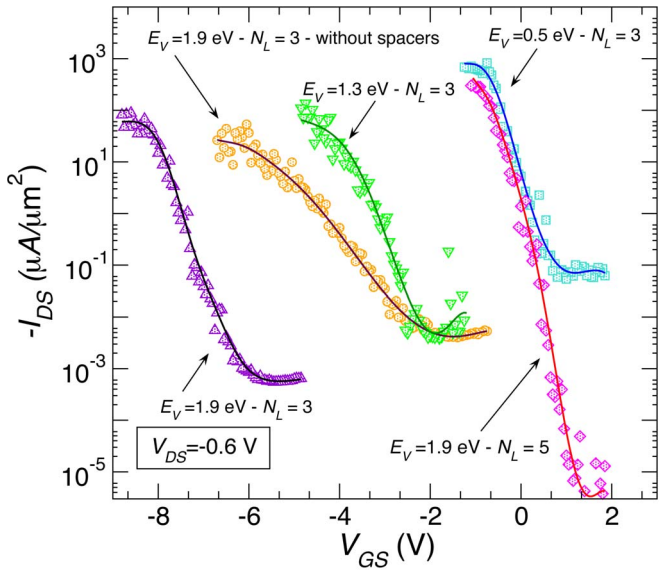

Figure 4 | (a) Transfer characteristics for the simulated VHFETs (EOT = 0.6 nm). The curves have been obtained by spline fitting the simulation data (symbols).

LHFET. We consider a LHFET with a p-type channel. The channel length is $L = 10$ nm and we consider a top and bottom gate aligned to the channel (see Figure 1 (c)), unless otherwise stated. The length of the p-doped source and drain extensions is set to 10 nm. The barrier region consists of a transversal strip of hBC_2N, that we model using the tight-binding parameters proposed in Ref. 23. In Figure 6 (a) we report the transfer characteristics corresponding to different choices of the length t_B of the barrier region. The curves look almost superimposed for $V_{GS} < -0.5$ V, while, for voltages closer to zero, the decrease in t_B entails a larger tunneling current component and, thus, an increase in the minimum of the current. SS_{min} settles to the almost ideal value of ≈64 mV/dec for $t_B > 7$ nm, gradually increasing for lower barrier thickness. Correspondingly, the I_{on}/I_{off} ratio rapidly decreases for $t_B < 4.5$ nm, while it shows slower variations for higher t_B (Figure 6 (b)). When t_B is increased beyond ≈8 nm, the PDP decreases as a result of the reduction of the fringe capacitances between the gates and the graphene channel: the overall variation in the PDP is however quite small (smaller than 30% for the considered t_B values). Apart from f_T, that reaches its maximum value for a barrier region slightly shorter than the channel, all the figures of merit are best for $t_B = L$.

As for the VHFET, we also investigated the influence of exploiting a different barrier material with different values for E_V. The plots in Figure 7 (a) and (b) show the behavior of the figures of merit as a function of E_V, assuming $t_B = 10$ nm. The points for $E_V =$

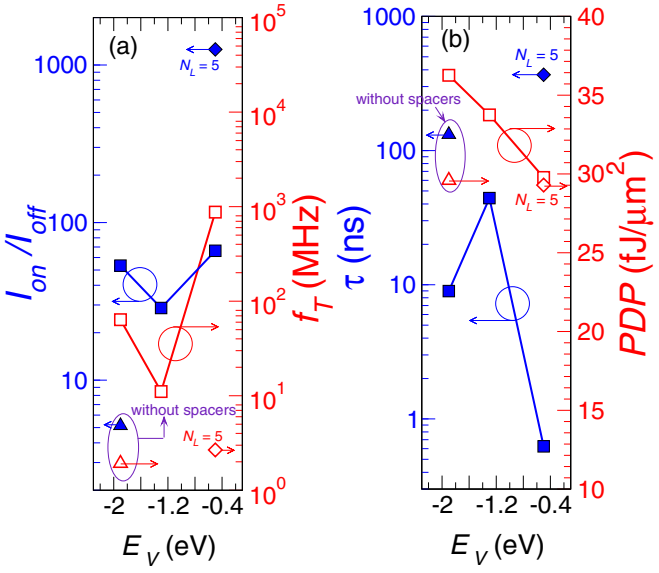

Figure 5 | Static and dynamic figures of merit for the simulated VHFETs. All data refer to $N_L = 3$, unless otherwise stated.

−0.642 eV refer to hBC_2N. We observe that a variation in E_V does not result just in a rigid shift in V_{GS} of the transfer characteristic, that would leave the I_{on}/I_{off} ratio unvaried. Indeed, jointly varying E_V and V_{GS} in order to keep constant the value of I_{DS} entails a variation in the perturbation of the potential of the source and drain region induced by the fringe field of the gate. This, in turn, modifies the exact shape and height of the barrier seen by holes near the interfaces with graphene, and therefore the current and carrier density modulation. The influence on the figures of merit is however only minor.

Discussion

The ITRS 2012 for high-performance logic MOSFETs[33] requires, at the 10 nm node (years 2020–2021), a I_{on}/I_{off} ratio of about 10^4. The Intrinsic Delay Time and the Power-Delay Product are required not to exceed 0.2 ps and 0.25 fJ/μm, respectively.

Both the barristor and the VHFET appear to be far from some of these targets, even in the optimistic case of our simulations. Concerning the barristor, we obtain a maximum I_{on}/I_{off} ratio as high as 10^6, but a minimum value for τ of ≈160 ps. Moreover, by setting to 10 nm one of the lateral dimension of the device, we obtain a minimum PDP of ≈6.7 fJ/μm. For the VHFET the best performance we obtained are: $I_{on}/I_{off} \approx 10^3$, $\tau \approx 600$ ps and PDP ≈ 0.3 fJ/μm.

On the positive side, the results obtained for the static and dynamic performance of the LHFET can fairly exceed the ITRS requirements: the 10-nm FET can exhibit a I_{on}/I_{off} ratio up to ≈3×10^4, a τ smaller than 0.05 ps and a PDP of ≈0.05 fJ/μm. Our results also predict a favourable scaling behavior, as can be inferred from Table 1, showing the results for the intrinsic delay corresponding to different gate lengths.

Concerning radio frequency operation, our results predict that the lateral FET could outperform by several orders of magnitude the vertical ones, potentially reaching intrinsic cutoff frequencies in the range of THz, beyond the highest measured values in MOSFETs[34], in high electron mobility transistors[35] and in graphene nanoribbon FETs[36].

We can gain insight into the discrepancy between the performance of the three devices by considering the plots in Figure 8. We call *gate control factor* (GCF) the derivative of the potential $\psi_B(V_{GS})$ of the

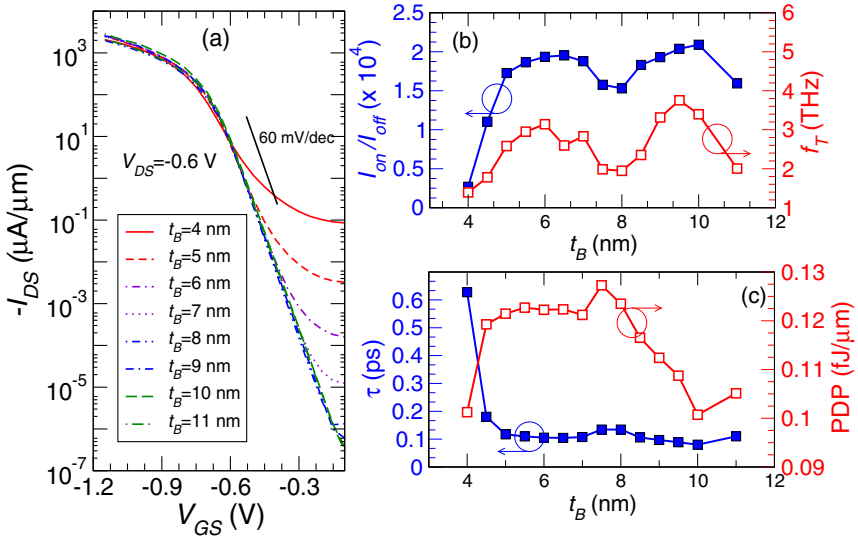

Figure 6 | (a) LHFET transfer characteristics for EOT = 1 nm and different values of t_B. (b), (c) Static and dynamic figures of merit extracted from the simulation data. Points for $t_B = 11$ nm refer to $L = 11$ nm (channel symmetrically extended on the drain and source side).

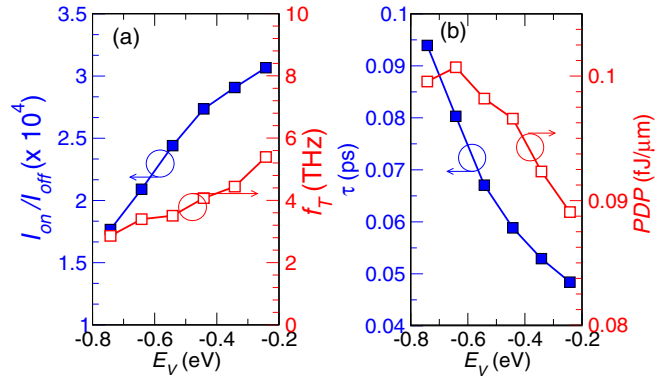

Figure 7 | Static and dynamic figures of merit for the simulated LHFETs, for EOT = 1 nm, t_B = 10 nm and different values of E_V.

edge of the barrier modulating the current with respect to V_{GS}. It is a measure of the effectiveness of the electrostatic control: GCF close to 1 corresponds to a perfect control of the gate(s) over the potential barrier.

We report in Figure 8 (a) the gate control factor and in Figure 8 (b) the relevant quantum capacitances[39] per unit area $C_Q = \partial\rho/\partial\psi$ as a function of V_{GS}, where ρ and ψ are the charge density and the electrostatic potential in the considered point of the device, respectively.

In the case of the barristor, the GCF appears narrow peaked. The correlation with the behavior of the quantum capacitance in graphene is apparent. The peak in GCF corresponds to the minimum in the C_Q plot, while its rapid falling off is related to the charge accumulation and increase in screening as C_Q increases. The high average value of quantum capacitance, entailing a rapid increase with V_{GS} of the charge in the device, limits high-frequency performance.

The VHFET shows a similar behavior, but with a wider and lower peak. We notice that, despite the double gate architecture, the maximum value in the GCF is close to that found in the barristor. We can explain these features by noticing that, since the Fermi levels in the upper and lower graphene channel differ because of the finite V_{DS}, the minimum in the quantum capacitance (Dirac point crossing the Fermi level) associated to them is achieved for different values of V_{GS}. This limits the maximum achievable GCF and broadens its peak.

In the case of the LHFET we face a quite different scenario. The key point is that now the effectiveness of the electrostatic modulation and the charge accumulation depend only on the properties of hBC_2N, since no overlap between gates and graphene is present ($t_B = L$). From Figure 8 we can see that the quantum capacitance of hBC_2N is negligible for $V_{GS} < 0.6$ V, when the device is in subthreshold regime. Corrispondingly, the GCF settles to ≈1, i.e. barrier height is perfectly controlled by the gate voltage. This allows to obtain an almost ideal subthreshold slope (*cf.* Figure 6).

Table 1 | ITRS 2012 requirements for the intrinsic delay time at different technological nodes, compared with representative values obtained from device simulation. Barristor: graphene/GaAs heterojunction with EOT = 0.6 nm and $N_D = 10^{18}$ cm^{-3}. VHFET: EOT = 0.6 nm, $E_V = -0.5$ eV and $N_L = 3$. LHFET: EOT = 1 nm, $E_V = -0.642$ eV and $t_B = L$

	Gate length		
	10 nm	7 nm	5 nm
ITRS 2012	0.17 ps	0.13 ps	–
LHFET	0.08 ps	0.05 ps	0.04 ps
VHFET	625 ps	625 ps	625 ps
Barristor	160 ps	160 ps	160 ps

Conclusion

We have performed fully quantum transport simulations of three recently proposed field-effect transistors based on lateral or vertical graphene heterostructures, in order to assess achievable device performance. For each device we have extracted the most significant figures of merit for different choices of the relevant physical parameters. Since our simulations refer to the optimistic case of defectless devices in which dissipative processes are confined to the contact reservoirs, our results represent an upper bound on the actual performance to be expected.

We found that only the lateral heterostructure FET has the potential to outperform both the ITRS requirements for CMOS technology at the 10 nm node and state-of-the-art devices for radiofrequency applications. On the other hand, transistors based on vertical heterostructures exhibit much worse performance, by at least three orders of magnitude in terms of intrinsic delay time and by at least two orders of magnitude in terms of transition frequency.

Very importantly from the point of view of industrial interest, the LHFET is also promising from the point of view of technology scaling, since its performance continues to improve for gate lengths down to 5 nm.

Methods

Device simulation has been performed by means of the open source package NanoTCAD ViDES[16,32], implementing the self-consistent solution of the Poisson and the Schrödinger equation within the Non-Equilibrium Green's Function formalism. Open boundary conditions have been considered for the Schrödinger equation at source and drain electrodes, corresponding to model the contacts with semi-infinite leads.

Two different approximations have been used for the Hamiltonian. In the case of barristor a one-dimensional two-bands $\mathbf{k}\cdot\mathbf{p}$ approximation along the transport direction has been considered. The presence of graphene has been accounted for by including in the self-consistent computation the sheet charge density obtained by integrating the $\mathbf{k}\cdot\mathbf{p}$ graphene density of state. The height of the Schottky barrier at the graphene/semiconductor interface has been approximated with the difference betweeen the graphene and semiconductor work function[18].

In the case of the VHFET and the LHFET the transport region has been modeled with a semi-empirical nearest-neighbor tight-binding approximation, assuming a perfect matching between the graphene and the insulator lattice. In detail, the layers composing the VHFET heterostructure have been assumed Bernal stacked, without any rotational misalignement[37,38].

In order to recast the three-dimensional problem into a two-dimensional one, the layered structures have been considered as infinitely extended in the transversal x direction (Figure 1 (b) and (c)). By exploiting the transverse translation symmetry, the Hamiltonian has been mapped into an effective two-dimensional one, parametrized in term of the transverse wave vector k_x[30]. Results for the local density of states and the transmission have been obtained by adding the contributions for different k_x in a large enough set within the first Brillouin zone.

Once obtained the self consistent Green's function of the system and extracted from it the transmission coefficient as a function of energy $\mathscr{T}(E)$, the current I has been computed by means of the Landauer formula

$$I = \frac{2e}{h}\int_{-\infty}^{\infty} \mathrm{d}E\, \mathscr{T}(E)\, \mathscr{F}(E), \tag{4}$$

where e is the electron charge and h the Planck constant. For our two-dimensional models the function $\mathscr{F}(E)$ reads

$$\mathscr{F}(E) = f(E - E_{FS}) - f(E - E_{FD}), \tag{5}$$

where $f(E)$ is the Fermi-Dirac distribution function, and E_{FS}, E_{FD} denote the Fermi level at the source and drain contacts, respectively. In the case of the one-dimensional model adopted for the barristor $\mathscr{T}(E)$ reads[40]

$$\mathscr{T}(E) = \frac{m_n^* K_B T}{\pi\hbar^2} \ln\left[\frac{1+\exp\left(\frac{E_{FD}-E}{K_B T}\right)}{1+\exp\left(\frac{E_{FS}-E}{K_B T}\right)}\right] \tag{6}$$

for the energies of electron propagating states, and

$$\mathscr{T}(E) = \frac{m_p^* K_B T}{\pi\hbar^2} \ln\left[\frac{1+\exp\left(\frac{E-E_{FS}}{K_B T}\right)}{1+\exp\left(\frac{E-E_{FD}}{K_B T}\right)}\right] \tag{7}$$

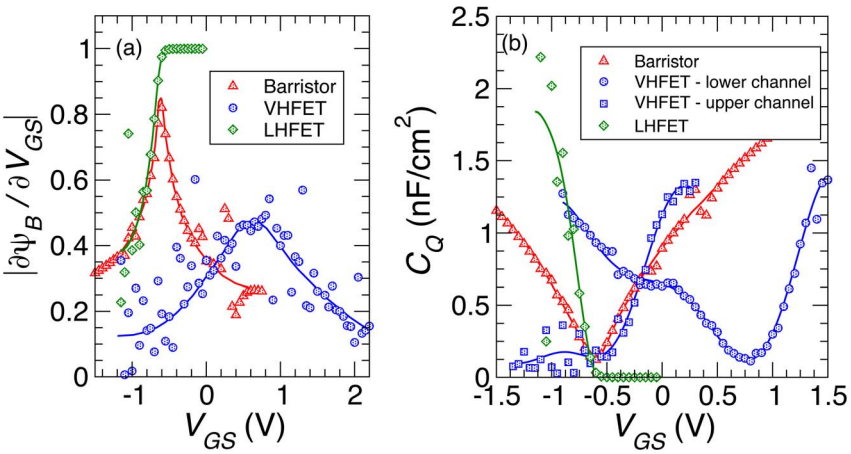

Figure 8 | (a) Gate control factor $|\partial\psi_B/\partial V_{GS}|$ as a function of V_{GS}. Barristor: graphene/GaAs heterojunction with EOT = 0.6 nm and $N_D = 10^{17}$ cm^{-3}. VHFET: EOT = 0.6 nm, $E_V = -0.5$ eV and $N_L = 5$. LHFET: EOT = 1 nm, $t_B = 10$ nm and $E_V = -0.642$ eV. (b) Quantum capacitance per unit surface as a function of V_{GS}, corresponding to the graphene regions of barristor and VHFET, and to the barrier region of LHFET. Data for the VHFET and LHFET refers to the y coordinate midway between that of the source and drain contact. Curves in both panels are guides for the eye.

for the energies of hole propagating states. We have denoted with K_B the Boltzmann constant, with $\hbar$ the reduced Planck constant and with m_n^*, m_p^* the effective masses (assumed isotropic) of electrons and holes, respectively.

In the case of the VHFET, our simulation results appear to be affected by higher levels of numerical noise with respect to the case of the barristor and the LHFET. This is mainly related to the presence in the VHFET simulation geometry of the transversal edges terminating the top and bottom graphene layer on the opposite side with respect to the source and drain contacts, respectively. Indeed, the charge and the current density in the neighborhood of these edges show a particularly strong dependence on the electrostatic potential, which makes considerably more involved the achivement of the Poisson-Schrödinger self-consistency and finally leads to the noisy dependence on the gate voltage of the current and the charge in the device.

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Author contributions

G.I. and G.F. conceived and developed the computer experiments and the models. G.F. developed and extended the code. D.L. run the numerical simulations and analysed the data. All authors discussed and interpreted simulation results. D.L. wrote the manuscript with contributions from the coauthors.

Additional information

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