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Current Saturation and Voltage Gain in Bilayer Graphene Field Effect Transistors

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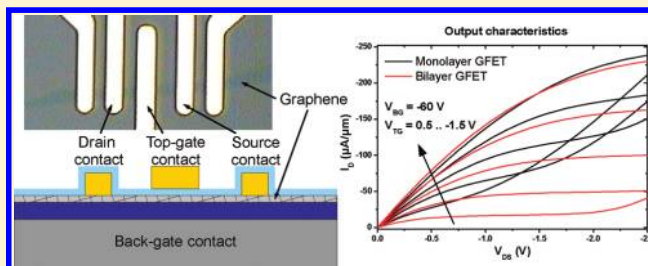
Supporting Information



ABSTRACT: The emergence of graphene with its unique electrical properties has triggered hopes in the electronic devices community regarding its exploitation as a channel material in field effect transistors. Graphene is especially promising for devices working at frequencies in the 100 GHz range. So far, graphene field effect transistors (GFETs) have shown cutoff frequencies up to 300 GHz, while exhibiting poor voltage gains, another important figure of merit for analog high frequency applications. In the present work, we show that the voltage gain of GFETs can be improved significantly by using bilayer graphene, where a band gap is introduced through a vertical electric displacement field. At a displacement field of −1.7 V/nm the bilayer GFETs exhibit an intrinsic voltage gain up to 35, a factor of 6 higher than the voltage gain in corresponding monolayer GFETs. The transconductance, which limits the cutoff frequency of a transistor, is not degraded by the displacement field and is similar in both monolayer and bilayer GFETs. Using numerical simulations based on an atomistic p_z tight-binding Hamiltonian we demonstrate that this approach can be extended to sub-100 nm gate lengths.

KEYWORDS: *Bilayer graphene, field effect transistor, graphene devices, current saturation, voltage gain*

The investigation of the ultimate potential and performance of graphene field effect transistors (GFET)[1−3] in radio frequency (RF) applications is currently one of the hot topics in the electrical engineering community.[4] Although the so far achieved cutoff frequencies f_T in GFETs up to 300 GHz are quite promising for future applications,[5−7] the fabricated devices show poor voltage gain. This could be a roadblock for their exploitation in RF electronics. The intrinsic voltage gain of a field effect transistor can be expressed by the transconductance g_m and the output conductance g_d. The former (g_m) is the derivative of the drain-current I_d with respect to the gate voltage and reflects the strength of current modulation in the channel by the gate voltage, while g_d, the derivative of the drain current by the drain voltage, represents the inverse of the output resistance of the transistor. The intrinsic voltage gain can then be expressed by the ratio $A_V = g_m/g_d$. In graphene very high values of g_m up to 5.9 mS/μm were already obtained,[8] while the weak current saturation yields g_d values comparable to g_m, leading to negligible voltage gain.[8] Therefore it is a major challenge to reduce g_d in GFETs, while preserving g_m.

Up to now, several papers have addressed the output conductance of GFETs, showing that a reduction of g_d can be achieved by increasing the gate coupling and by optimizing the interface between the graphene and the dielectric layers,[9−11] which eventually led to A_V close to 10. Although such results are quite promising, they are still far from performance requirements for future RF devices, where A_V = 30 is targeted for devices with sub-100 nm gate length.[12] The introduction of a small band gap in graphene was already proposed as possible solution to reduce the output conductance and to increase the voltage gain of GFETs.[13] Additionally, a reduction of the ouput conductance would also improve the thermal stability of a graphene based RF circuit.[14] In the present work we have taken this concept and explore the possibility of exploiting bilayer graphene in order to obtain GFETs with large A_V. In bilayer graphene the application of a perpendicular electric displacement field leads to a tunable band gap reaching values up to 300 meV.[15−19] So far, this approach has been adopted to modulate the channel resistance in double- and single-gated bilayer GFETs[20−22] and to realize logic gates based on double-gated bilayer GFETs,[23,24] while an improved current saturation has been observed in bilayer GFETs only at liquid nitrogen temperatures (77 K).[24]

To investigate the effect of the band gap opening in bilayer GFETs on the output characteristics and the voltage gain, we have fabricated double-gated mono- and bilayer GFETs on a Si/SiO_2 substrate with Ni contacts, an Al_2O_3 top-gate dielectric, and a Ti/Ni top-gate electrode.

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Highly p-doped Si wafers covered with 90 nm thermally grown SiO_2 were used as a substrate. Prior to the graphene deposition, the substrate was coated with hexamethyldisilazane (HMDS) in a chemical vapor deposition process to make the SiO_2 substrate highly hydrophobic and reduce the hysteresis and intrinsic doping concentration of graphene based FETs.[25] Subsequently, the graphene was exfoliated with an adhesive tape from a natural graphite crystal and deposited on the substrate. The layer number of the graphene flakes was identified using optical microscopy and contrast determination of the graphene relative to the substrate.[26] For several flakes, also Raman spectroscopy has been applied for verification.[27] After graphene deposition, the contact electrodes were fabricated by photolithography, sputter deposition of 40 nm nickel and a subsequent lift-off process. The top-gate dielectric was deposited by thermal evaporation of 1 nm Al serving as a seed layer for the subsequent atomic layer deposition of 10 nm Al_2O_3.[28] This resulted in an equivalent oxide thickness of 8 nm. The top-gate electrode consisting of 5 nm Ti and 40 nm Ni was defined with photolithography, sputter deposition, and lift-off. Ti has been chosen as the lower metal layer, because the work function mismatch between Ti and graphene leads to a slight n-type doping of the graphene channel.[29] An optical micrograph of a fabricated device is depicted in the inset of Figure 1. The

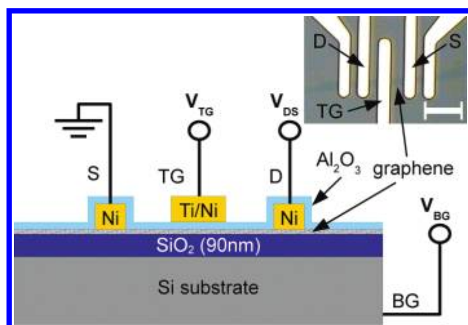

Figure 1. Experimental setup. Schematic of a double-gated GFET and the corresponding measurement setup used in our experiments. Inset: Optical micrograph of a double-gated bilayer GFET. The scale bar is 10 μm.

gate length of all devices (2 monolayer and 3 bilayer GFETs) is 4 μm and the graphene channel width ranges from 4 to 9 μm. The length of the ungated graphene channel is 3 μm on each side of the top-gate electrode. We note that the charge carrier density and thus the resistance of the ungated graphene channel is strongly influenced by the applied back-gate voltage. All samples were measured in a needle probe station in nitrogen atmosphere at room temperature after an in situ annealing at 200 °C for one hour. For electrical characterization, a HP 4156 semiconductor parameter analyzer was used. The top-gate, source, and drain electrode were contacted using needle probes, and the back-gate voltage was applied to the substrate through the sample carrier. The sample has been biased as illustrated in Figure 1.

In the bilayer GFETs, the energy gap is manifested by a decrease of the minimum channel conductivity with increasing back-gate voltage V_{BG} from −10 to −60 V. This results in an increased current modulation up to a value equal to 30, which is about a factor of 10 larger than the current modulation in the monolayer GFETs (see Supporting Information). From the transfer characteristics we have determined the field effect mobility. In the monolayer it is 2200 $cm^2/(Vs)$ while in the bilayer it is 2000 $cm^2/(Vs)$. These values are comparable with results shown in the literature for monolayer[6,10] and bilayer devices.[21,30]

In Figure 2a,b, we show the output characteristics for a monolayer and a bilayer GFET at a back-gate voltage of −60 V.

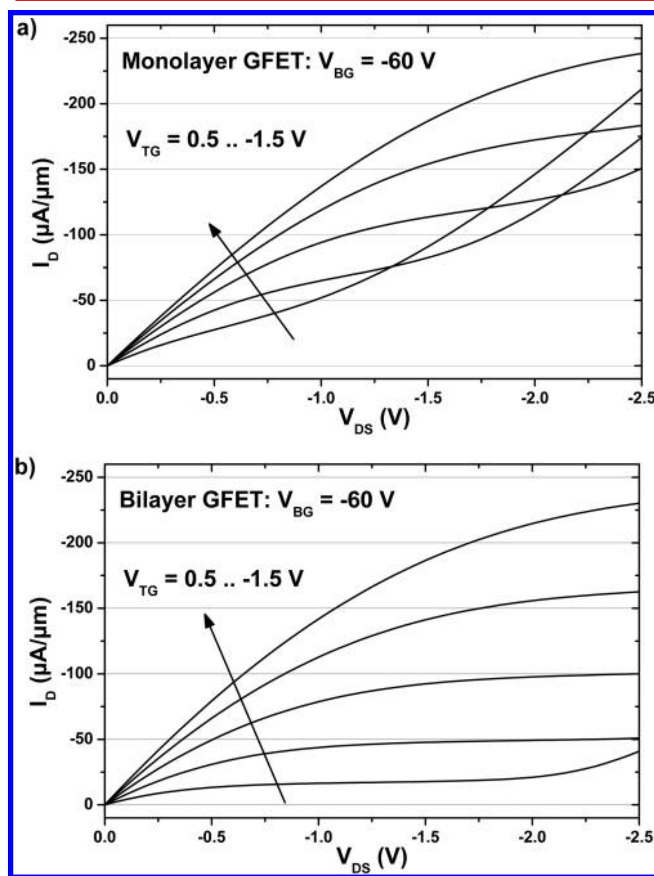

Figure 2. Output characteristics. Current as a function of the source-drain voltage of (a) a monolayer GFET and (b) a bilayer GFET at a back-gate voltage V_{BG} = −60 V. The top-gate voltage V_{TG} ranges from −1.5 to 0.5 V with 0.5 V steps.

The back-gate displacement field is around −1.7 V/nm. This vertical displacement field introduces an electrically effective gap of approximately 80 meV in the bilayer graphene. Details on the calculation of the displacement field and the estimation of the energy gap are given in the Supporting Information. As can be seen in Figure 2, drain-current saturation is much more pronounced in the bilayer GFET compared to the monolayer GFET, where the lack of a band gap does not allow a proper pinch-off of the channel.[31] The corresponding output conductance is by a factor of 10 smaller in the bilayer GFET compared to the monolayer GFET (0.002 and 0.02 mS/μm, respectively). Furthermore, drain-current saturation in the bilayer GFET is observable in a wider V_{DS} range and at lower drain current densities. These improvements lead to a higher thermal stability and a lower power consumption compared to a monolayer GFET.[14]

Current saturation in field effect transistors can be either due to electrostatic pinch-off of the channel or to velocity saturation of the charge carriers.[32] In the first case, transconductance is linear with the gate voltage, while in the second case it remains constant. In our monolayer GFET, the S-shape output characteristic is due to a local pinch-off of the channel as

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previously shown by Meric et al.[31] For the bilayer GFET case instead, we have verified a linear dependence of g_m on V_{TG} (see Supporting Information). Therefore, we can conclude that the reduced output conductance in the bilayer GFET has to be imputed to an improved pinch-off of the channel, due to the electrostatically induced band gap.

To investigate in more details the effect of the applied back-gate voltage on the minimum output conductance (i.e., the influence of a band gap on the current saturation), we plot in Figure 3 g_d as a function of V_{BG} for the monolayer and the bilayer GFET. The data of all investigated devices is included in the Supporting Information. As can be seen, g_d in the monolayer GFET depends only weakly on the applied back-gate voltage, while a reduction by an order of magnitude can be observed in the bilayer device, when decreasing V_{BG} from −10 to −60 V. This behavior is a clear signature of band gap opening in bilayer graphene for increasing vertical displacement field. The observed minimum output conductance in the monolayer GFETs is in the range of 0.02 to 0.05 mS/μm, which is in agreement with results shown for other monolayer GFETs.[6−11] At V_{BG} = −60 V, the minimum output conductance in the bilayer GFETs is by a factor of 10 smaller in the range of 0.002 to 0.004 mS/μm.

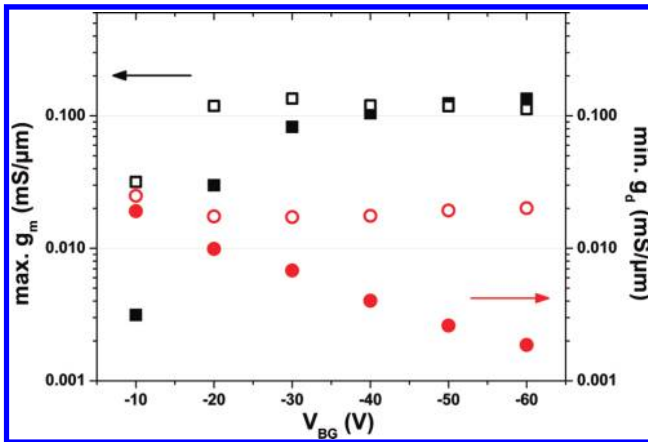

Figure 3. Maximum values of the transconductance g_m (squares) and minimum values of the output conductance g_d (circles) as a function of the applied back-gate voltage V_{BG} for a monolayer (open symbols) and a bilayer GFET (filled symbols).

Figure 3 also shows the maximum transconductances g_m for the monolayer and bilayer GFET as a function of the back-gate voltage. For small V_{BG} from −10 to −20 V, we observe for both devices an initial increase of g_m, which can be related to the reduction of the resistance in the ungated graphene channel by the applied V_{BG}. At larger V_{BG} (−30 to −60 V), we cannot observe a clear dependence of g_m on the applied V_{BG}. Furthermore, the transconductance g_m shows a similar behavior in the monolayer and the bilayer GFET. These findings can provide relevant information combined with the cutoff frequency f_T, which can be expressed in the quasi-static approximation as $f_T = g_m/(2\pi C_G)$, where C_G is the gate capacitance. Since the transconductance g_m does not degrade with increasing vertical displacement field, we can state that an improvement of the output conductance does not degrade f_T, as also demonstrated theoretically.[14]

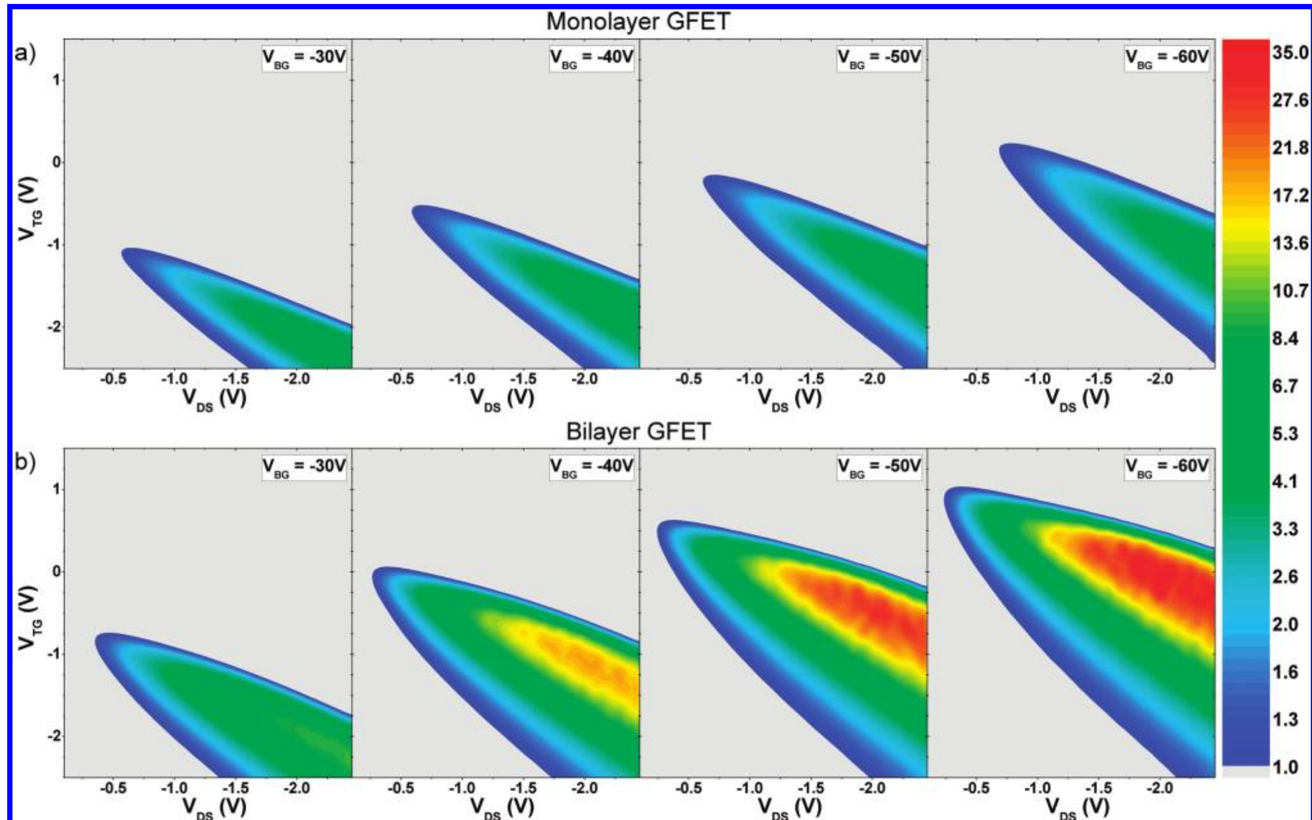

Figure 4. Contour plots of the voltage gain versus source-drain and top-gate voltage in a monolayer (a) and a bilayer GFET (b). The plots were calculated from the measured output characteristics at different applied back-gate voltages from −30 V (left) to −60 V (right). The voltage gain is color-coded in logarithmic scale.

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The voltage gain A_V extracted from the output and transfer characteristics for the mono- and bilayer GFETs is plotted in Figure 4 as a function of V_{TG} and V_{DS} for different back-gate voltages; the light gray region refers to $A_V < 1$. We observe that for the monolayer GFET the maximum value of A_V is 6 independent of the V_{BG}, while for the bilayer GFET the A_V increases from 10 at $V_{BG} = -30$ V to 35 at $V_{BG} = -60$ V. Also, voltage gain is observed on a wider voltage region for bilayer than for the monolayer GFET. For both cases, the maximum shifts toward the top of the $V_{TG}-V_{DS}$ plane for negatively increasing V_{BG} that is due to the induced Fermi level shift within the channel. We conclude that the increase in voltage gain is a direct consequence of the reduction of the output conductance in the bilayer GFET, when increasing the applied negative back-gate voltage. The very same behavior has been observed in all the investigated samples, that is, three bilayer and two monolayer GFETs.

Parasitic effects like charge traps can distort a correct measurement of the output characteristics and even lead to a negative g_d.[31] In those cases, g_m/g_d does not reflect the intrinsic voltage gain properly. To check wether such effects compromise our measurements, we also have directly measured the voltage gain of a bilayer GFET integrated in a simple circuit. The measured voltage gain of the circuit was in excellent agreement with the values calculated from g_m and g_d (see Supporting Information). Thus, we are convinced that $A_V = g_m/g_d$ reflects the intrinsic voltage gain of the investigated devices and is not affected by parasitic effects.

The fabricated devices with a gate length of 4 μm have rather large dimensions compared to state-of-the-art FETs, which have gate lengths in the submicrometer regime. In order to understand if drain-current saturation and voltage gain can still be observed in ultrashort channel devices, we have performed accurate numerical simulations based on an atomistic p_z tight-binding Hamiltonian. To this purpose, we have made extensive use of the open-source code NanoTCAD ViDES,[33] and we have performed simulations based on the self-consistent solution of the 2D Poisson and the Schroedinger equation with open boundary conditions, within the non-equilibrium Green's function (NEGF) formalism. Details on the simulations are given in the Supporting Information. The simulations show that improved output characteristics can still be observed for bilayer GFETs but not in monolayer GFETs, even when considering a short gate length of 40 nm. The simulated bilayer GFET shows a voltage gain of up to 10, while the monolayer device does not show any voltage gain ($A_V < 1$). Such differences have to be attributed to the induced band gap in bilayer GFETs. The simulations demonstrate that using monolayer graphene without a band gap might be a road block for analog high frequency applications, where a voltage gain is required. Bilayer graphene with a band gap offers instead a viable option.

In summary, we have demonstrated that GFETs with a bilayer graphene channel are more suitable to achieve excellent current saturation and voltage gain. Thus, bilayer GFETs might show a higher thermal stability and reduced power consumption compared to monolayer devices. The main reason is the decreasing output conductance with increasing band gap in the bilayer graphene. Furthermore, we showed that the theoretical cutoff frequency f_T is not influenced by the opening of the band gap. Through numerical simulations we demonstrated that current saturation and voltage gain can still be achieved in ultrascaled bilayer GFETs.

■ ASSOCIATED CONTENT

Supporting Information

Top- and back-gate transfer characteristics including comments on current modulation. Output characteristics at lower back-gate voltages. Dependence of the transconductance versus top-gate voltage in the saturation regime. Minimum output conductance and maximum transconductance of all investigated devices. Estimation of the maximum displacement field and the maximum energy gap. Comparison of calculated and measured voltage gain. Details on the simulations including device parameters, output characteristics, and voltage gain. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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