

Ultralow-Voltage Bilayer Graphene Tunnel FET

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Abstract—In this letter, we propose the bilayer graphene tunnel field-effect transistor (TFET) as a device suitable for fabrication and circuit integration with present-day technology. It provides high $I_{\text{on}}/I_{\text{off}}$ ratio at ultralow supply voltage, without the limitations in terms of prohibitive lithography and patterning requirements for circuit integration of graphene nanoribbons. Our investigation is based on the solution of the coupled Poisson and Schrödinger equations in three dimensions, within the non-equilibrium Green's function formalism on a Tight Binding Hamiltonian. We show that the small achievable gap of only few hundreds of millielectronvolts is still enough for promising TFET operation, providing a large $I_{\text{on}}/I_{\text{off}}$ ratio in excess of 10^3 even for a supply voltage of only 0.1 V. A key to this performance is the low quantum capacitance of bilayer graphene, which permits to obtain an extremely small subthreshold swing S smaller than 20 mV/dec at room temperature.

Index Terms—Bilayer graphene, low-power device, non-equilibrium Green's function (NEGF), tunnel field-effect transistor (TFET).

I. INTRODUCTION

VERY recent theoretical and experimental papers [1]–[4] have shown the possibility of inducing an energy gap (E_{gap}) in bilayer graphene by means of an applied electric field perpendicular to the graphene plane. This property could open the possibility of fabricating carbon-based electron devices, for which a semiconducting gap is required, with state-of-the-art lithography. Let us stress that the alternative option of inducing a gap by means of lateral confinement to fabricate graphene nanoribbon field-effect transistors (FETs) [5] requires single-atom control and prohibitive lithography to define widths close to 1 nm [6].

Since the largest attainable E_{gap} in bilayer graphene is of few hundreds of millielectronvolts, band-to-band tunneling strongly limits device performance, so that the $I_{\text{on}}/I_{\text{off}}$ ratio of the drain current is typically smaller than 10 [7].

One can, however, turn this limitation into an advantage, fully exploiting band-to-band tunneling instead of avoiding it, like in tunnel FETs (TFETs), which have been widely

investigated in the past through experiments and simulations, considering different channel materials [8]–[10].

The main appeal of TFETs is the possibility of obtaining a subthreshold swing S well below that obtained in conventional FETs, which would in turn allow one to strongly reduce the supply voltage for digital logic well below 0.5 V, and consequently the power consumption [8].

In this regard, it has been recently observed [11] that 1-D carbon-based devices are more promising than planar silicon devices, because of the small carrier effective mass that enhances the I_{on} current, and of the small quantum capacitance in the ON-state, which guarantees good electrostatic control of the channel through the gate voltage, improving S .

In this letter, we propose the realization of an ultralow-power bilayer graphene TFET (BG-TFET) and investigate its performance by means of numerical simulations based on the self-consistent solution of the 3-D Poisson and Schrödinger equations, within the nonequilibrium Green's function (NEGF), implemented in our open source code NanoTCAD ViDES [12].

We show that a large $I_{\text{on}}/I_{\text{off}}$ ratio in excess of 10^3 can be obtained for a voltage V_{DD} of only 0.1 V. The low quantum capacitance of bilayer graphene allows us to grab the advantages provided by 1-D carbon channels also with a planar—more easily manufacturable—structure, and to achieve very low S .

II. RESULTS AND DISCUSSION

The Schrödinger equation has been solved within a p_z orbital basis set in the real space. Implementation details can be found in [7] and [13].

The device structure is shown in Fig. 1(a). The considered device is a double-gate BG-TFET, driven by two independent gates, biased with voltages V_{top} and V_{bottom} . The channel length L is 40 nm, and the p^+ and n^+ reservoirs are 40 nm long and doped with molar fraction f . The bilayer graphene is embedded in a 3-nm-thick SiO_2 insulator with relative dielectric constant $\epsilon_r = 3.9$. A gate overlap has also been taken into account, whose effects will be discussed later on.

In Fig. 1(a), a band edge profile of the TFET in the OFF-state is also shown. Since the potential in the vertical direction falls linearly, the device is in the OFF-state (minimum current in the channel) for $V_{\text{bottom}} = V_{\text{min}} \equiv (V_{\text{top}} - V_{\text{bottom}})/2 + V_{\text{DS}}/2$, where V_{DS} is the drain-to-source voltage.

The conduction and valence bands can be divided in five subregions along the transport direction: the source, the so-called virtual source, the channel, the virtual drain, and the drain. Deep in the source and drain regions, the conduction and the valence bands coincide because the vertical electric field rapidly goes to zero. A gap is induced in all the regions

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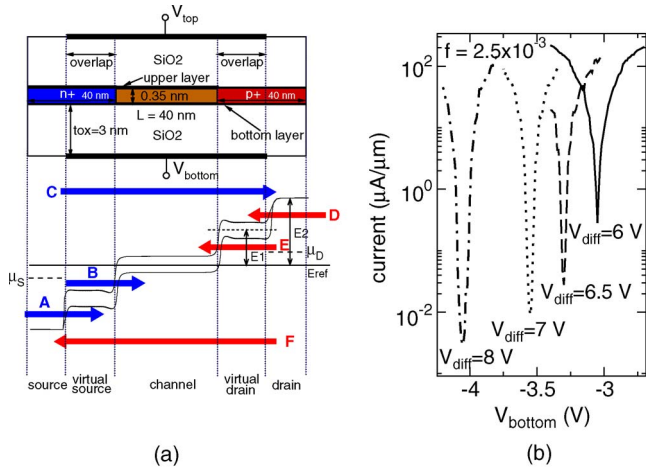


Fig. 1. (a) Sketch of the double-gate bilayer graphene TFET: the channel length is 40 nm, and n^+ and p^+ reservoirs are 40 nm long with molar fraction f . The device is embedded in a 3-nm-thick SiO_2 dielectric. V_{top} and V_{bottom} are the voltages applied the top and bottom gate, respectively. Gate overlap has been also considered. Below, band edge profile of the device in the OFF-state. (b) Transfer characteristics of the double-gate BG-TFET for different V_{diff} . f is equal to 2.5×10^{-3} and $V_{\text{DS}} = 0.1$ V.

surrounded by the top and the bottom gates, where a differential voltage $V_{\text{diff}} \equiv V_{\text{top}} - V_{\text{bottom}}$ is imposed, i.e., in the virtual source and drain regions and in the channel.

Six different fluxes of carriers contribute to transport, identified with a letter in Fig. 1(a): tunneling electrons (A and B fluxes), tunneling holes (E and D fluxes), and thermally emitted electrons (C) and holes (F). In order to obtain a small I_{off} , all mentioned fluxes have to be minimized through proper band engineering.

One solution could be inducing a large energy gap, which translates in imposing a large vertical electric field. This option is, however, limited by the breakdown field of the oxide, and by the gate leakage current. To this purpose, we have chosen SiO_2 as a gate dielectric, which guarantees an intrinsic breakdown field close to 14 MV/cm [14] (well above the simulated vertical electric fields), and a large graphene/ SiO_2 band offset (larger than 3 eV), which ensures very small gate leakage currents.

The molar fraction of the source and drain leads instead determines E_1 and E_2 , the difference between the midgap potential in the channel (E_{ref}) and the midgap in the virtual drain and in the drain, respectively (same considerations obviously follow for the source): the higher f , the higher E_1 and E_2 . Decreasing E_1 and E_2 can help in reducing E and D (or A and B in the source), but in turns increases of thermionic emission (C and F).

Let us focus on the performance of the BG-TFET with ultralow supply voltage $V_{\text{DD}} = 0.1$ V. In Fig. 1(b), we show the transfer characteristics as a function of V_{bottom} of a device with molar fraction $f = 2.5 \times 10^{-3}$, for fixed differential gate voltages $V_{\text{diff}} = 6, 6.5, 7$, and 8 V.

As can be noted, differently from what happens in double-gate BG-FETs [7], the BG-TFET can be perfectly switched off, with a steep subthreshold behavior (always smaller than 20 mV/dec) and a large $I_{\text{on}}/I_{\text{off}}$ ratio also for a very low V_{DD} (e.g., $I_{\text{on}}/I_{\text{off}} = 4888$ for $V_{\text{diff}} = 8$ V).

TABLE I

$I_{\text{on}}/I_{\text{off}}$ RATIOS, E_{gap} COMPUTED IN THE MIDDLE OF THE CHANNEL \mathcal{E} , THE ELECTRIC FIELD IN THE MIDDLE OF THE CHANNEL, AND SUBTHRESHOLD SWING S FOR DIFFERENT V_{diff}

V_{diff} (V)	$I_{\text{on}}/I_{\text{off}}$	E_{gap} (eV)	\mathcal{E} (MV/cm)	S (mV/dec)
6	147	0.24	9.45	21
6.5	885	0.25	10.23	13
7	2822	0.260	11.02	12
8	4888	0.274	12.59	14

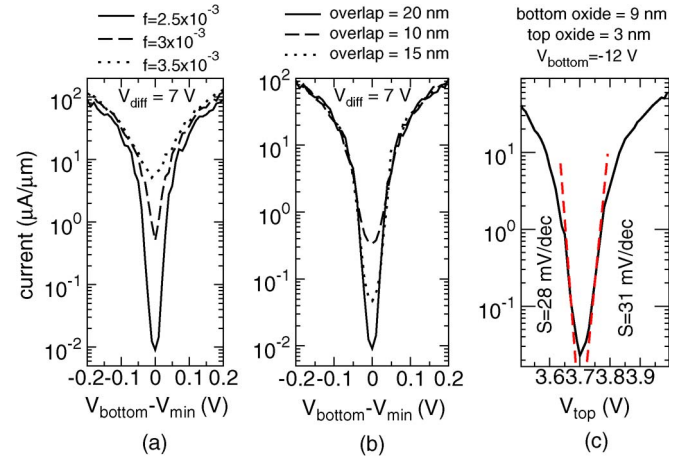


Fig. 2. (a) Transfer characteristics of BG-TFETs for $V_{\text{diff}} = 7$ V, $V_{\text{DS}} = 0.1$ V, and different molar fractions f . $V_{\text{min}} = -3.55$ V. (b) Transfer characteristics of BG-TFET for $V_{\text{diff}} = 7$ V, $V_{\text{DS}} = 0.1$ V, and different gate overlap. $V_{\text{min}} = -3.55$ V. (c) Transfer characteristic for a device with asymmetric oxide thicknesses: The top oxide thickness is 3 nm, and the bottom oxide thickness is 9 nm. V_{bottom} is fixed to -12 V and $V_{\text{DS}} = 0.1$ V.

The capability of electrostatically tuning the energy gap can be fully exploited in BG-TFET, as shown in Table I, where $I_{\text{on}}/I_{\text{off}}$ increases by a factor of 33, varying V_{diff} from 6 to 8 V, as also experimentally demonstrated in [15].

Due to the large vertical electric field, particular attention has also to be posed on the gate leakage current. We can estimate its value using a well-tested analytical model for Si– SiO_2 gate stacks based on WKB approximation of the triangular barrier [16]. We find that 3-nm gate oxide is sufficient to obtain a gate current of the order of 10^{-6} $\mu\text{A}/\mu\text{m}$ for $V_{\text{diff}} = 7$ V, and 10^{-4} $\mu\text{A}/\mu\text{m}$ for $V_{\text{diff}} = 8$ V, i.e., negligible with respect to the smallest drain currents considered in our simulations.

In Fig. 2(a), we show the transfer characteristics as a function of V_{bottom} , for $V_{\text{diff}} = 7$ V, and for different dopant molar fractions f in the drain and source leads. As f is increased, the $I_{\text{on}}/I_{\text{off}}$ ratio degrades, since I_{off} increases, while I_{on} remains almost constant.

In Fig. 2(b), we show the transfer characteristics as a function of gate overlap. As shown, the smaller the overlap, the higher the I_{off} current, since it is the energy gap of the virtual reservoirs that suppresses tunneling from contacts to the channel.

In order to investigate the performance of single-gate devices, we have also performed simulations of a device with asymmetric gate oxide thicknesses [Fig. 2(c)]: the top oxide is 3 nm, and the bottom oxide is 9 nm. In this case, the bottom gate voltage is kept at a constant bias of -12 V, whereas the top gate is used as the control gate. This solution, with a common back gate at constant voltage for all FETs, is obviously more suitable for circuit integration.

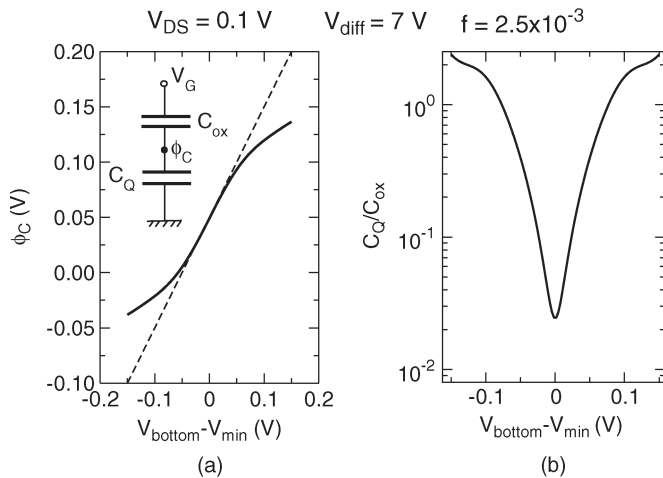


Fig. 3. (a) (Solid line) Electrostatic potential in the middle of the channel ϕ_C as a function of the bottom gate voltage. The dashed line refers the case in which the gate control is ideal, i.e., $\phi_C = (V_{\text{bottom}} - V_{\text{min}}) + V_{\text{DS}}/2$. In the inset, the equivalent capacitance circuit of the device is shown. (b) Ratio of the quantum capacitance C_Q and the oxide capacitance C_{ox} .

As can be noted, an $I_{\text{on}}/I_{\text{off}}$ ratio of few hundreds can be still obtained. The subthreshold swing (and then the $I_{\text{on}}/I_{\text{off}}$ ratio) can be improved with a thicker bottom oxide of the order of 100 nm, which would reduce the capacitive coupling between channel and bottom gate. We, however, limited our analysis to 9 nm, because of numerical convergence problems encountered when dealing with larger structures.

As noted in [11], 1-D channels are typically more appealing for tunneling device applications than planar 2-D channels, since their quantum capacitance C_Q is smaller than the electrostatic capacitance C_{ox} even in the ON-state. Such condition guarantees a good gate control over the potential barrier and larger $I_{\text{on}}/I_{\text{off}}$.

In Fig. 3(a), we show ϕ_C , the electrostatic potential in the middle of the channel, as a function of the bottom gate voltage, for $f = 2.5 \times 10^{-3}$ and $V_{\text{diff}} = 7$ V. On the same plot, we also show the line $\phi_C = V_{\text{bottom}} - V_{\text{min}} + V_{\text{DS}}/2$, corresponding to ideal control of the channel potential from the gate voltage. As shown, also for larger gate voltages, ϕ_C reasonably follows V_{bottom} , and no channel potential saturation is observed. As indeed shown in Fig. 3(b), where the ratio C_Q/C_{ox} is depicted, for small voltages the device is working in the Quantum Capacitance Limit (i.e., $C_Q \ll C_{\text{ox}}$), whereas for larger values C_Q is comparable with C_{ox} . However, it never reaches the condition $C_Q \gg C_{\text{ox}}$ as in silicon TFETs. As a consequence, despite its bidimensionality, bilayer graphene is appealing for tunneling devices applications.

III. CONCLUSION

In conclusion, we have performed a numerical analysis of a BG-TFETs, based on the self-consistent solution of the 3-D

Poisson/Schrödinger equations, within the NEGF formalism. Large $I_{\text{on}}/I_{\text{off}}$ ratios can be obtained even for an ultralow supply voltage of only 100 mV, thanks to an extremely steep subthreshold slope. The low quantum capacitance of bilayer graphene allows the BG-TFET to have most of the advantages of 1-D TFETs, but none of the disadvantages in terms of structure patterning and lithography. Indeed, since present-day lithography is adequate for the fabrication of BG-TFETs, and the single-gate driving option with constant bottom gate bias is suitable for planar integration, we consider the device very promising for fabrication experiments and circuit integration.

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