Two dimensional Graphene/h-BCN based devices with large Ion/Ioff ratio for digital applications

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Abstract. We present a performance assessment of graphene/hexagonal Boron Nitride heterojunctions based transistors able to provide large current modulation. The study is performed by means of a multi-scale approach leveraging ab-initio simulations to capture the physics at the atomic scale, and tight-binding simulations to compute transport. In particular, we focus on two technological solutions, a vertical and a planar structure both able to provide large Ion/Ioff ratios. As we will show, due to reduced capacitative coupling, the planar structure outperforms the vertical device as far as digital applications are concerned.

Introduction

Despite the outstanding electrical properties of graphene [1,2], there is a roadblock to its exploitation in electronic applications, due to the lack of a band-gap, which prevents to completely switch-off the channel as desired in digital electronics.

The scenario would drastically change, if we could find a way to block one of the main stream of the particles, either electrons or holes. To this purpose, we will focus on two technological options, one based on a planar structure [3] and one on a vertical structure [4], which indeed allow the suppression of the band-to-band tunneling component of the current, when the device is in the off-state.

In particular, the planar structure we proposed have been triggered by a paper by Ci et al. [5] and it is based on two-dimensional graphene intercalated with h-BCN (hexagonal boron carbon nitrogen). The vertical structure has been instead demonstrated experimentally to allow large current modulation, but an extensive performance analysis against ITRS requirements [6] has not been addressed so far.

We will show that while planar heterostructure device shows performance complying with ITRS requirements, the vertical structure device has poor performance due to the large capacitative coupling.

Methods

The self-consistent solution of the 2D Poisson and Schrödinger equation has been performed within the NEGF formalism. In particular, a tight-binding p_z orbital basis set in the real space has been adopted for the Hamiltonian in order to compute the charge and the transport along the graphene based channel. Within a multi-scale approach, semi-empirical tight-binding parameters have been extracted from DFT calculations.

Ab-initio calculations have been performed by means of the Quantum Espresso code [7], using a plane wave basis set in the generalized gradient approximation (GGA) with the Perdew-Burke-Ernzerhof (PBE) exchange correlation functional. A 50 Ry wave function cutoff and 400 Ry charge

density cutoff have been considered, while the Brillouin zone has been sampled using a 30x30x2 Monkhorst Pack grid. A 30 bohr layer of vacuum is considered to separate the sheet from its periodical images, which we have verified to be sufficient to avoid any unphysical interactions. The geometries are fully relaxed without any symmetry constraints, while the convergence of the total energy and force are set to 1×10^{-7} Ry/au.

The obtained energy dispersion relations have been then fitted to extract the tight-binding parameters and to accurately reproduce the bottom of the conduction band and the top of the valence band. To this purpose, our open-source device simulation package NanoTCAD ViDES [8] has been extensively exploited to evaluate device operation through the self-consistent solution of the 2D Poisson and the Schrödinger equation with open boundary conditions, within the non-equilibrium Green's function (NEGF) formalism.

The ballistic conductance has been calculated by means of the PWCOND module [9] of Quantum Espresso. The transport properties are studied in the framework of Landauer-Büttiker formalism, where the total transmission at energy E is obtained as the sum over the transmission probability of the conducting eigenchannels, averaged over the two-dimensional Brillouin zone normal to the transport direction.

Results

As recently demonstrated experimentally in [5], large current modulation can be obtained in a vertical structure as the one shown in Fig. 1a. In particular, two graphene flakes are separated by a dielectric (in this case h-BN) and connected to two independent gates. A top and bottom gate instead allow the modulation of the channel barrier. The simulated device is a p-MOS Field Effect Transistor, with top and bottom high-k gate dielectrics (i.e. HfO_2 with relative dielectric constant equal to 25) with thickness of 4 nm. Top and bottom metallic gates are driven by the same voltage V_{GS}. Different numbers of h-BN layers have been taken into account, in order to investigate the effect of barrier thickness on device electrical properties (Fig. 1a).
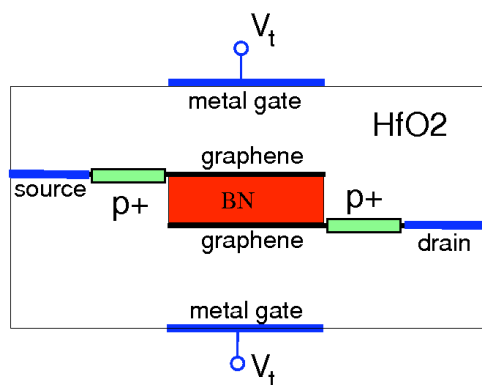

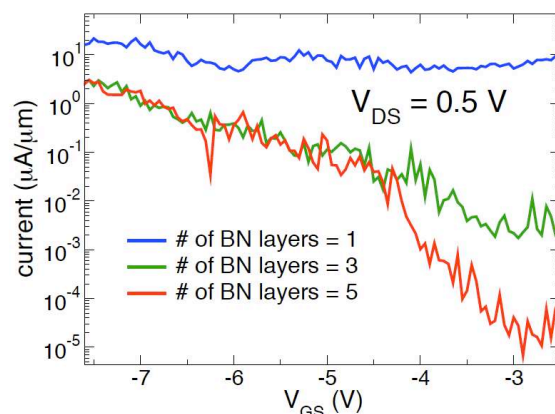Fig. 1a: Longitudinal cross-section of the vertical transistor.

Fig. 1b: Transfer characteristics of the vertical transistor for different number of BN layers.

In Figure 1b, we show the drain current I_{DS} as a function of the gate voltage, for a drain voltage of 0.5 V (source is grounded) and for a different number of h-BN layers (i.e. 1,3 and 5). As can be seen, the 1-layer h-BN barrier has no current blocking properties, whereas the 3- and 5-layer h-BN allow a current modulation of five orders of magnitude. For $V_{GS} < -4.5V$, current is independent of the number of layers, which means it is essentially of thermionic nature.

The serious problem, from the application viewpoint, is that large current modulation occurs over several volts, which prevents the use of the proposed device for digital applications.

Indeed, the sub-threshold swing (SS) is of the order of 300 mV/dec, much worse than that attainable in double gate MOSFET, i.e. really close to the ideal SS=60 mV/dec. Such poor performances has to be attributed to the large capacitative coupling between the two flakes, the flakes and the gate, and the flake and the ground, i.e. the quantum capacitance.

In Fig. 2, we show another technological solution, where the parasitic capacitances are reduced, and allowing the block of the band-to-band tunneling component of the electron in the off-state by means of the lateral h-BCN barrier. In particular, the planar graphene-based FET has an h-BCN barrier of thickness t_B in the graphene channel, exactly below the gates. Two metallic gates have a length $L > t_B$ and therefore overlap on the graphene regions, and are separated from the channel by a silicon oxide layer of thickness 1 nm. Three different h-BCN composites have been considered, and in particular, h-BN, h-BC$_2$N and h-BC$_6$N. h-BCN material possesses the interesting property of a bandgap, which can be modulated through changing the C concentration: the larger the C concentration, the smaller the energy bandgap.

Graphene regions below the gate are undoped, whereas those forming the source and drain extensions are doped with donors or acceptors for obtaining nFETs or pFETs, respectively.
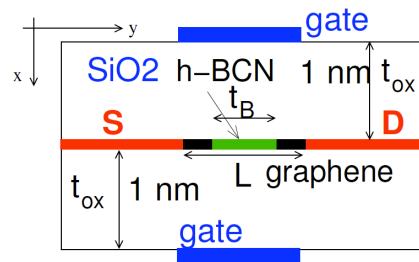
Fig.2: Longitudinal section of the considered h-BCN based graphene transistor. Source and drain reservoirs are doped with a molar fraction f. Within the graphene channel, a h-BCN barrier t_B-thick has been considered.

The corresponding transfer characteristics for p-type FETs are shown in Fig. 3. As a reference, the transfer characteristics of a graphene FET (GFET) is also shown (black dashed line Fig 3a). As can be seen, the introduction of a h-BCN barrier in the middle of the channel improves the Ion/Ioff ratio with respect to that of a simple GFET, which is smaller than 10.

For the BC$_2$N case, an Ion/Ioff ratio larger than 10^4 can be obtained, complying with ITRS requirements for next technological nodes. Such devices can manage to reach the THz range, if other parasitics are kept under control.
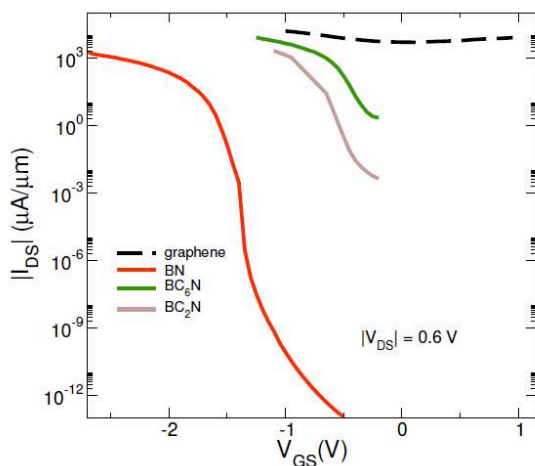
Fig.3a: Transfer characteristics for the different barrier materials. All the considered devices are p-MOS. f = 10−2 or BC_2N and BC_6N. f = 5 x 10^{-2} for BN. t_B=5 nm.
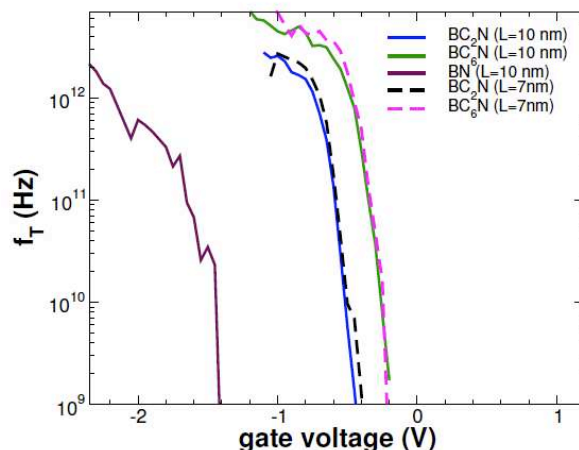
Fig. 3b: Cut-off frequency defined as f_T = $g_m/2C_G$, where g_m is the channel transconductance and C_G the gate capacitance, as a function of VGS for the different h-BCN barriers.

Summary

Through a multi-scale approach based on ab-initio simulations and tight-binding semi-empirical Hamiltonian, we have investigated the performance of graphene/hBN heterostructure based device. In particular, a planar and a vertical structure have been considered against ITRS requirements. Simulations have shown that while both structures manage to modulate the current among several orders of magnitude, the planar structure offers better perspectives as compared to the vertical structure, due to the reduced parasitic coupling between the channel and the overlaying gates.

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