Bilayer Graphene Transistors for Analog Electronics

Gianluca Fiori, Daniel Neumaier, Bart N. Szafranek, and Giuseppe Iannaccone, *Senior Member, IEEE*

***Abstract*— In this paper, we investigate with theory and experiments the performance improvements achievable using bilayer graphene as channel material in field effect transistors for analog applications. Bilayer graphene provides larger output resistance than monolayer graphene, which translates in both higher voltage gain and higher maximum frequency oscillation. To experimentally prove bilayer graphene potential as a channel material, simple circuits have been fabricated and tested, i.e., an amplifier and a frequency doubler. We show that they largely outperform similar circuits built with monolayer-graphene devices.**

***Index Terms*— Current saturation, frequency doubler, graphene, graphene amplifier, NEGF.**

I. Introduction

ANALOG applications are considered with increasing interest for graphene-based transistors, as they seem to harness graphene's most promising properties, the ultrahigh mobility and the large saturation velocity, without suffering from the absence of a bandgap [1]–[3].

In analog electronics the field effect transistors (FETs) are biased in inversion and therefore one can try to take full advantage of high mobility to reach large transconductance g_m and high transition frequency f_T.

So far graphene transistors have delivered f_T of 427 and 300 GHz at gate lengths of 67 and 140 nm, respectively [4], [5]. These values are significantly larger than corresponding f_T obtained from silicon transistors and comparable with those of the best III/V semiconductor transistors [6].

However, the absence of a bandgap in graphene has a negative impact also in analog applications. In short-channel devices, where transport is quasi-ballistic and drift velocity saturation does not occur, interband tunneling suppresses current saturation and therefore the intrinsic voltage gain $A_{v0} = g_m/g_0$, where g_0 denotes the output conductance. The lack of current saturation can be detrimental for f_{MAX}, the maximum oscillation frequency.

Recently, we have demonstrated with experiments and simulation that lower g_0 and larger A_v can be obtained by using bilayer graphene [7]. The reason is that by applying an electric field perpendicular to the bilayer graphene plane it is possible to induce a gap of 100–200 meV [8]–[12]. Such a small gap significantly improves the current saturation.

Here, we provide an extensive theoretical and experimental investigation of bilayer graphene FET for analog applications. First, we show how bilayer graphene can boost device performance when used in state-of-the-art devices [1], [13], by means of atomistic simulations based on tight-binding calculations. To this aim, we will use our open source device simulator NanoTCAD ViDES [3], [14], based on the self-consistent solution of the 3-D Poisson and of the Schrödinger equations with an atomistic tight binding Hamiltonian, within the nonequilibrium Green's functions formalism (NEGF). This approach will provide us physical insights on bilayer graphene FET operation. We will then experimentally demonstrate that bilayer graphene can represent a viable option for analog electronics, with the fabrication and the characterization of two electronic circuits, i.e., an amplifier and a frequency doubler.

Systems like frequency multipliers are key components for mobile communication systems. In frequency doublers, only the second harmonic is desired and sophisticated filtering techniques are required to suppress spurious harmonics. For graphene FETs (GFET) the ambipolar and symmetric transfer characteristics offer the possibility to create a second harmonic signal with an excellent spectral purity of more than 90% without additional filtering elements [15]–[17]. However, the obtained gain for the second harmonic is rather poor, reaching values of only up to -26 dB [17] and -16 dB in small bandgap carbon nanotube [18]. We show that using bilayer graphene as FET channel material can provide better performance in terms of voltage and second harmonic gain, with respect to monolayer-graphene FETs.

II. Physics of Bilayer Graphene FET

Here, we want to investigate the physics behind the mechanisms inducing current saturation in bilayer graphene FET, and provide design guidelines to obtain large voltage gain. The simulation approach is based on the self-consistent solution of the 2-D Poisson and transport equation within the NEGF formalism, implemented in the open-source code NanoTCAD ViDES. Transport has been assumed to be ballistic.

We will focus on the 40-nm device considered in the experiments in [1] [Fig. 1(a)], from which we draw general considerations, which also hold for long-channel devices.

The bottom dielectric layer consists of diamond-like carbon $t_{\mathrm{ox}} = 40$ nm, the top dielectric layer is Al_2O_3 with thickness equal to 20 nm.

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G. Fiori is with the Dipartimento Ingegneria dell'Informazione, University of Pisa, Pisa 56122, Italy (e-mail: gfiori@mercurio.iet.unipi.it).

D. Neumaier and B. N. Szafranek are with the Advanced Microelectronic Center Aachen, AMO GmbH, Aachen 52074, Germany (e-mail: neumaier@amo.de; szafranek@amo.de).

G. Iannaccone is with the Dipartimento Ingegneria dell'Informazione, University of Pisa, Pisa 56122, Italy, and also with the IEIIT CNR, Pisa 56122, Italy (e-mail: giuseppe.iannaccone@unipi.it).

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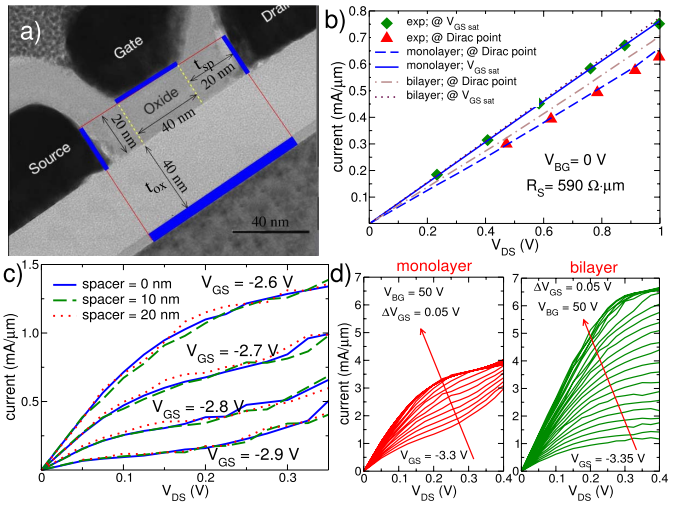

Fig. 1. (a) Device structure of [1], (top) oxide $t_{ox} = 20$ nm, and (bottom) oxide $t_{ox} = 40$ nm, spacer $t_{sp} = 20$ nm. (b) Comparison of experimental (points) and theoretical output characteristics (lines) considering $R_S = 590\ \Omega\cdot\mu$m for two different values of V_{GS}: source Fermi level at the Dirac point (at Dirac point) and $V_{GS} = V_{GSsat}$ when current saturates as a function of V_{GS} (at V_{GSsat}). (c) Simulated output characteristics of FET with $t_{ox} = 4$ nm, $t_{box} = 40$ nm, lateral spacer $t_{sp} = 0, 10, 20$ nm, backgate voltage $V_{BG} = 40$ V, bilayer graphene channel. The spacer has no effect. (d) Output characteristics of FET with $V_{BG} = 50$ V with monolayer graphene channel (left) and bilayer graphene channel (right).

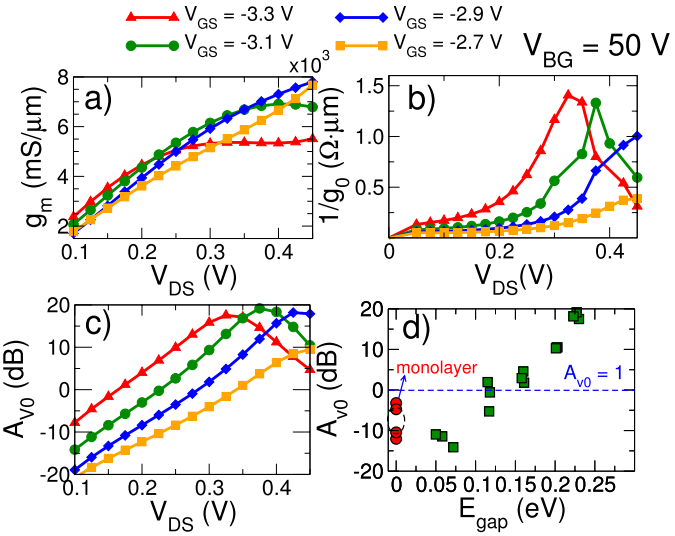

Fig. 2. (a) Transconductance, (b) output resistance, and (c) voltage gain as a function of V_{DS} for different V_{GS} and $V_{BG} = 50$ V. (d) Intrinsic gain A_{v0} as a function of E_{gap} for different V_{GS}.

Fig. 1(b) shows the measured output characteristics (dots) of the device shown in Fig. 1(a), when the channel is biased at the Dirac point and when current saturates as a function of V_{GS}, i.e., when further increase of V_{GS} does not lead to further appreciable increase of the current. By comparing the experiments with simulations (lines) performed with NanoTCAD ViDES, we can extract the contact resistance at source and drain $R_S = 590\ \Omega\cdot\mu$m, which is in good agreement with values extracted in experiments [19].

As one can observe in Fig. 1(b), the device exhibits very poor output characteristics for three main reasons: 1) poor current saturation; 2) large contact resistance; and 3) poor electrostatics due to large top/bottom oxide thickness ratio.

To understand the potential device performance and the improvements achievable with some bandgap engineering, we can slightly modify the structure shown in Fig. 1(a) by substituting the monolayer graphene with bilayer graphene, and by applying a significant vertical electric field to the channel. To do so, we apply a large positive voltage V_{BG} on the backgate and, to improve electrostatics, we reduce the top oxide thickness t_{ox} to 4 nm.

The output characteristics computed with $V_{BG} = 40$ V, for different values of the spacer layer t_{sp}, are shown in Fig. 1(c). As can be observed, good saturation of the output characteristics is obtained. From these results, we understand that the spacer is not a critical design parameter, since for this geometry the channel is more strongly coupled with the top and bottom gates, rather than with the lateral source and drain contacts.

To isolate and understand the improvements due to only bilayer graphene, we can consider the comparison in Fig. 1(d) between the output characteristics of two identical devices, biased with $V_{BG} = 50$ V, where the only difference is the use of monolayer graphene or bilayer graphene as channel. One can observe the much improved current saturation and transconductance provided by bilayer graphene, even with a small bandgap (0.22 eV).

For the same device and same backgate voltage, we show the transconductance, the inverse of the output conductance and the intrinsic gain $A_{v0} = g_m/g_0$ in Fig. 2(a)–(c), as a function of V_{DS} and for different V_{GS}.

One can observe that for $V_{GS} \leq -3.1$ V — for which we obtain the larger maximum A_{v0} — g_m saturates at large V_{DS} and $1/g_0$ has a narrow peak as a function of V_{DS}, which leads to the same behavior in A_{v0}. While the maximum intrinsic gain is promising, the fact that A_{v0} is not constant for the considered bias region can cause distortion in the amplification or a reduced effective gain. From Fig. 1(d), we note, however, that such distorsion is going to be much more pronounced in monolayer graphene since the V_{DS} window for which the current saturates is wider in bilayer than in monolayer-graphene FETs. This issue will be investigated in detail in the experimental section, addressing the harmonic distortion in the amplifier and in the frequency doubler.

Fig. 2(d) show that the energy bandgap is the main factor responsible for the high intrinsic gain achievable with bilayer graphene: the larger the bandgap, the larger the intrinsic gain.

Let us now consider the mechanisms leading to the improved current saturation. In Fig. 3, we show the conduction and valence band edges (yellow lines), and the color map of the current spectral density for different bias points (the brighter the color, the larger the current density). We note two main contributions to the total current: a thermionic component at energy higher than the conduction band edge, and a band-to-band-tunneling component at energy lower than the valence band edge. If the bandgap is too small, as in Fig. 3(a), both thermionic and tunneling components are relevant.

If we increase the backgate voltage, the gap increases and interband tunneling is suppressed, as shown in Fig. 3(b). In Fig. 3(c), we show the output characteristic for

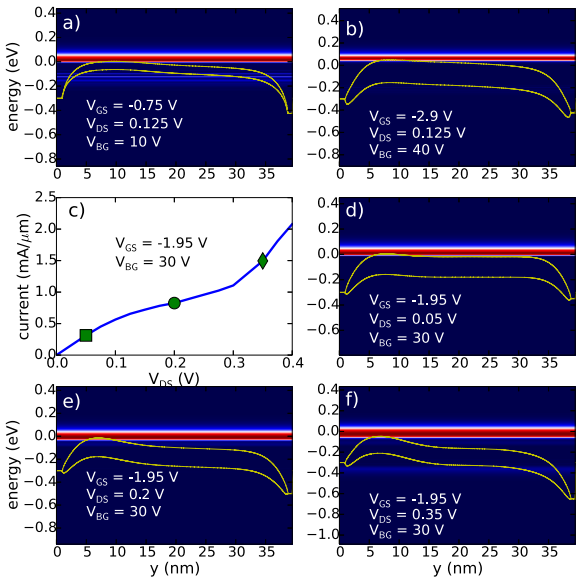

Fig. 3. Color plot of the current density of the bilayer graphene FET for different bias points. (a) Gap is too small due to the low V_{BG} so that we observe interband tunneling, which is suppressed in (b). (c) V_{DS} is so large the interband tunneling sets in. (d) Current saturates as a function of V_{GS} due to limited injection from the source.

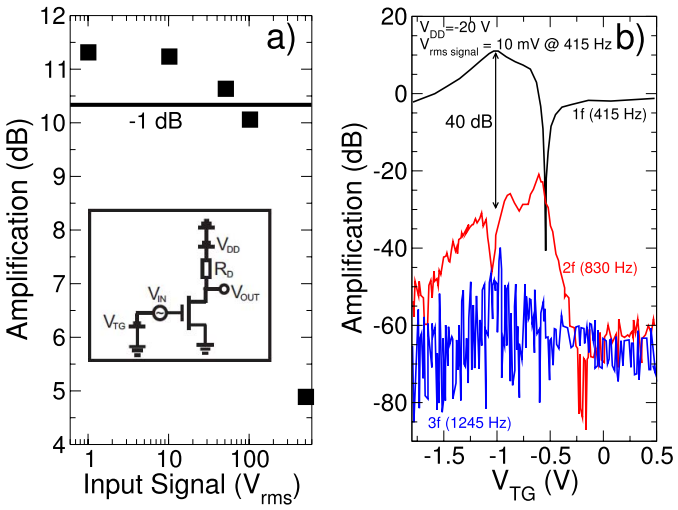

Fig. 4. (a) Amplification as a function of the rms input voltage. (b) Harmonic distorsion.

$V_{GS} = -1.95$ V and $V_{BG} = 30$ V, where three biasing points ($V_{DS} = 0.05$, 0.2 and 0.35 V) are highlighted, and corresponding bands profile are shown in Fig. 3(d)–(f), respectively. If the bandgap is sufficiently large to suppress band-to-band tunneling, the output characteristics resemble those of a classical MOSFET, where the thermionic current is predominant. In particular, for small V_{DS} the FET is in the linear regime [Fig. 3(d)], while for larger V_{DS} current saturates [Fig. 3(e)]. If V_{DS} is further increased, the band-to-band tunneling component is no more negligible, and current increases again [Fig. 3(f)].

As a design guideline, the tunneling current can generally be neglected as far as the applied V_{DS} times the elementary charge q is smaller than the induced bandgap.

III. Device Fabrication

We have fabricated double-gated bilayer GFETs by photolithography on Si wafers covered with 90 nm thermally grown SiO_2. Prior to the graphene deposition, the substrate has been coated with hexamethyldisilazane in a chemical vapor deposition process [20]. Subsequently, the graphene has been exfoliated with an adhesive tape from a natural graphite crystal and deposited on the substrate. The layer number of the graphene flakes has been identified using optical microscopy and contrast determination of the graphene relative to the substrate [21]. After graphene deposition, the contact electrodes have been fabricated by sputter deposition of 40-nm nickel and a subsequent lift-off process. The top-gate dielectric has been defined by thermal evaporation of 1 nm Al serving as a seed layer for the subsequent atomic layer deposition of 10 nm Al_2O_3 [22].

The top-gate electrode consists of 5-nm Ti and 40-nm Ni deposited by sputtering. The gate length of the investigated device is 4 μm, the channel width is 5 μm, and the distance between the source and drain electrodes is 9 μm.

IV. Bilayer Graphene Amplifier

As mentioned in the previous section, the narrow peak of the voltage gain might represent an issue for what concerns distortion of the amplifier output. Here, we investigate the harmonic distortion of a purposely fabricated bilayer-graphene FET amplifier, shown in the inset of Fig. 4(a).

A top-gate voltage (V_{TG}) is applied to induce a vertical electric field and a bandgap. The input signal V_{IN} is placed in series to V_{TG}. On the drain side, we have a load resistance R_D and the supply voltage generator V_{DD}.

The voltage gain $A_v = V_{OUT}/V_{IN}$ is measured for a back-gate voltage $V_{BG} = -60$ V as a function of V_{TG} and V_{DD} and depends on the intrinsic voltage gain as

$$A_v = A_{v0}\frac{g_0 R_D}{1 + R_D g_0} \tag{1}$$

where $R_D = 28$ kΩ.

As already demonstrated in [7], the intrinsic voltage gain in bilayer graphene FET is significantly larger than in state-of-the-art devices using monolayer graphene, i.e., $A_v = 3$ in [23] and $A_v = 5$ in [24].

As shown in Fig. 4(a), the 1-dB compression point is comparable with published results on monolayer graphene (i.e., [25] 1-dB compression point close to 60 mV), while the measured harmonic distortion [Fig. 4(c)] shows that the contribution of the second harmonic is negligible and smaller than 40 dB smaller than the first harmonic.

V. Bilayer Graphene Frequency Doubler

A promising application of graphene transistors is represented by frequency doublers. Indeed, when biasing GFETs at the charge neutrality point, the I–V relation is nearly quadratic, enabling frequency doubling with excellent spectral purity without using additional filters [15]. Such a quadratic

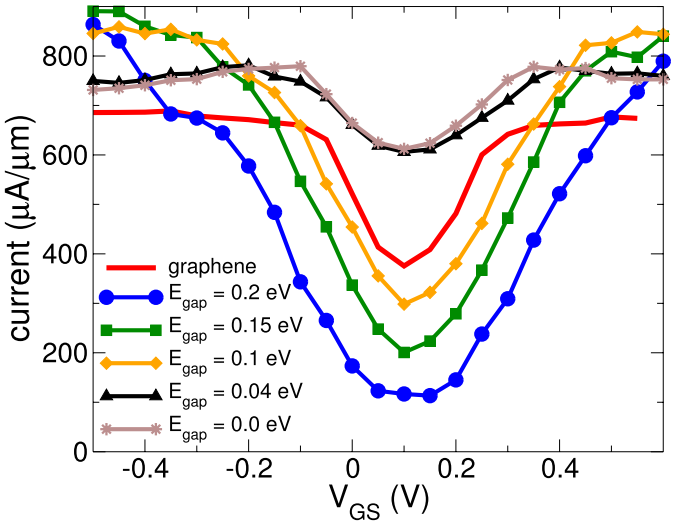

Fig. 5. Simulated transfer characteristics of bilayer graphene FET for different electrically induced bandgap. The transfer characteristics of a monolayer graphene FET is shown for comparison.

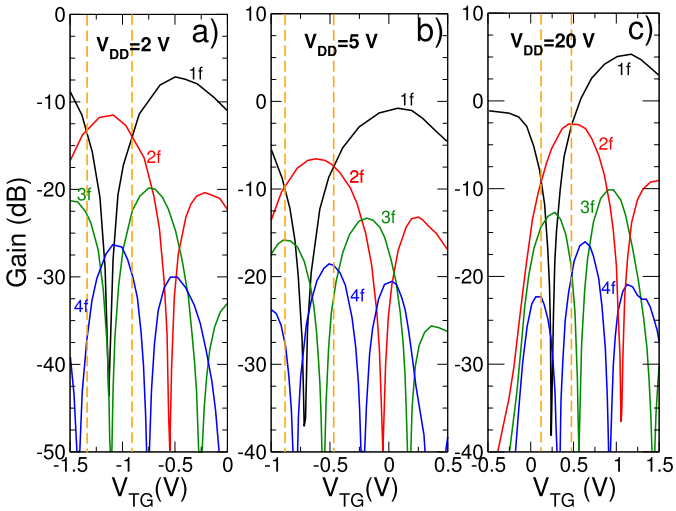

Fig. 6. Voltage gain for different harmonics (nf in the figure indicates the nth harmonic) of the input frequency 415 Hz as a function of the applied top-gate voltage V_{TG} for applied supply voltage V_{DD} of (a) 2, (b) 5, and (c) 20 V displayed in (a)–(c) respectively.

dependence is apparent in Fig. 5, where the transfer characteristics of bilayer graphene FET obtained from simulations for different induced bandgap energy are shown.

As can be observed, increasing the bandgap leads to an improved and more extended parabolic profile of the transfer characteristics as compared with monolayer graphene FET (red line) around the ambipolar turning point. This translates in better performance in terms of the purity of the harmonic component, i.e., in a larger second harmonic, compared with the first and higher order harmonics [18].

To prove the potential of bilayer graphene for frequency multipliers applications, we have fabricated frequency doublers with unprecedented quality of the induced second harmonic. We used the same device and circuit described in the previous section, where V_{IN} is a sinusoidal input with root mean square (rms) amplitude of 500 mV and frequency f_1 of 415 Hz, and the load resistance $R_D = 33$ kΩ. The output voltage V_{OUT} has been measured with a lock-in amplifier at different harmonics of the input frequency. The gain A_v for the first four harmonics is plotted as a function of V_{TG} in Fig. 6 for a supply voltage V_{DD} of 2 V [Fig. 6(a)], 5 V [Fig. 6(b)], and 20 V [Fig. 6(c)]. For all the considered V_{DD} we observe a region of V_{TG} bias where the second harmonic is much larger than the first, third, and fourth harmonics (area delimited by vertical orange dashed lines), roughly corresponding to the case in which Fermi energy in the graphene channel is close to midgap. For $V_{DD} = 2$ V, the voltage gain for the second harmonic is -12 dB with 95% of the overall ouput power. Increasing the power supply leads to an increase of the gain for the second harmonic.

The obtained results represent a significant improvement with respect to the state of the art. In Fig. 7, we plot the maximum relative power concentrated at the second harmonic for different V_{DD} as a function the corresponding voltage gain for the presented frequency multiplier and for the latest results from the literature based on monolayer graphene [16], [17], [26], [27] and on carbon nanotubes [18]. Additionally, at low

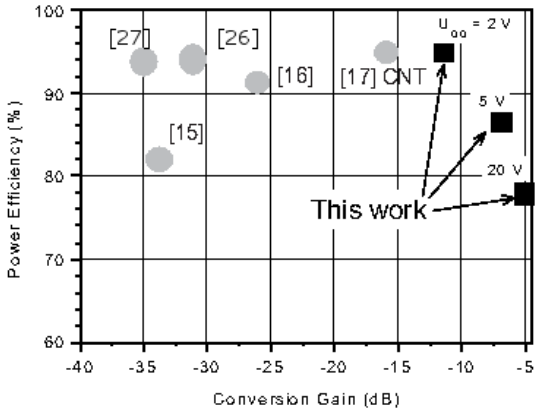

Fig. 7. Relative power at the second harmonic as a function of the corresponding voltage gain. The results obtained in the present work are compared with state-of-the-art results from the literature.

V_{DD} the increase in gain does not result in a reduction of the relative power concentrated at the second harmonic frequency.

An increase of V_{DD} leads to larger second harmonic gain, but also reduces the spectral purity. This trend is already visible in Fig. 6 and has its origin in the I–V characteristics getting more and more asymmetric due to the applied supply bias. However, even for the highest V_{DD} considered here the spectral purity is still much better than those in conventional frequency multipliers based on diodes and transistors, due to the ambipolar FET behavior.

VI. Conclusion

In conclusion, we have demonstrated the advantages of using bilayer graphene as FET channel in transistor figures of merit, in amplifiers, and frequency doublers. We have gained from numerical simulations physical insights on the mechanisms providing larger A_v than monolayer-graphene FETs, i.e., the electrostatically-induced bandgap of up to 220 meV, sufficient to suppress interband tunneling and provide accept-

able output resistance. The induced bandgap also improves the parabolic profile of the transfer characteristics around the ambipolar turning point, which can be exploited in frequency doublers.

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Gianluca Fiori is an Assistant Professor with the University of Pisa, Pisa, Italy. He is the leading developed of the open-source code NanoTCAD ViDES. His current research interests include the simulation of 2-D material based transistors and the performance assessment of novel nanoscale devices.

Daniel Neumaier received the Ph.D. degree in physics from TU Munich, Munich, Germany, and the University of Regensburg, Regensburg, Germany, in 2009.

He has been the Head of the Graphene Group, AMO GmbH, Aachen, Germany, since 2009. From 2006 to 2009, he was with the Group of Dieter Weiss, University of Regensburg, involved in III/V spintronics. His current research interests include graphene based devices for high-frequency electronic, optoelectronic, and sensor applications.

Bart N. Szafranek, photograph and biography not available at the time of publication.

Giuseppe Iannaccone (M'98–SM'10) is a Professor of electronics with the University of Pisa, Pisa, Italy. He has co-authored more than 160 papers in peer-reviewed journals and 120 papers in proceedings of international conferences. His current research interests include nanoelectronics and quantum transport, design of nanopower analog integrated circuits, RFID, and smart systems.