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Geometrical Effects on Valley-Orbital Filling Patterns in Silicon Quantum Dots for Robust Qubit Implementation

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The effect of the geometrical confinement on the shell filling in quantum dots obtained in silicon-on-insulator (SOI) tri-sided gate metal oxide semiconductor single-electron transistors (MOSSETs) is investigated on the basis of the current spin density functional theory. Variations of the geometric shape in nanowire SOI-MOSSETs with square section entail important changes in the valley filling sequences, whereas the variability of the gate length does not imply a significant modification of the filling patterns. Our results provide quantitative insights towards the shell engineering of silicon quantum dots for qubits with stable valley filling patterns.

We discuss the geometrical effects on the energy states in single quantum dots obtained in silicon-on-insulator (SOI) tri-sided gate metal oxide semiconductor single-electron transistors (MOSSETs) in order to design robust valley-irrespective qubits in silicon quantum dots. Silicon quantum dots have been proposed and used[1)] to implement qubit architectures.[2–5)] A robust implementation of a qubit exploiting the physical properties of confined electrons in a single quantum dot fabricated in silicon nanostructures should take into account the complexity of silicon valley physics.[6–8)] Moreover, orbital states associated with different types of valleys have to be under control even when the valley degree of freedom is not exploited in the quantum computation. Different approaches for creating single-electron silicon quantum dots have been explored, including the employment of gate-induced two-dimensional electron gas (2DEG) at the Si/SiO_2 interfaces,[9)] global gate-controlled edge roughness of an ultra small nanowire,[10)] local gate-equipped underlap geometry where the gate is not at the state of the art and consequently enforces the use of large gate voltages,[11)] triple-layer gate stacks,[6)] Si/SiGe modulation-doped heterostructures,[12)] SOI metal oxide semiconductor field-effect transistors with an additional upper gate[13)] and SOI tri-sided gate MOSSETs.[14–16)]

In the past, we have applied the current spin density functional theory (CS-DFT) for determining the electron localization in complementary MOS (CMOS)-compatible single-electron devices.[16)] CS-DFT returns the ground state of the system by minimizing the energy as a functional of the charge density, spin density, and paramagnetic current density. Such a method is suitable to investigate devices carrying a complex structure and involving a high number of electrons. Here, CS-DFT is used to investigate the geometrical effects on the filling of valley states in single quantum dots. The SET is modeled as a silicon nanowire, as shown in Fig. 1, with length L along the x-direction and by a rectangular section in the y–z plane with width W and silicon thickness T_{Si} on the top of a silicon dioxide slab of thickness $T_{box} = 45$ nm. The device has a tri-sided gate structure with gate length L_g, and the gate is insulated from the nanowire with a $T_{ox} = 4$-nm-thick silicon dioxide layer. Source and drain metal contacts are the y–z planes at the head and tail of the nanowire. Spacers of length $L_{sp} = 15$ nm between the source/drain contact and the edge of the triside gate are present. We used a modified version of the three-dimensional self-consistent simulator based on CS-DFT in the framework of the NanoTCAD ViDES package.[17–19)] It solves the many-body Schrödinger equation using CS-DFT in the local density approximation and in the effective mass approximation with parabolic bands in each of the three families of Δ valley pairs along the three different directions in the k space, providing the ground state of the system for each occupation number N of electrons. The Kohn–Sham equation reads

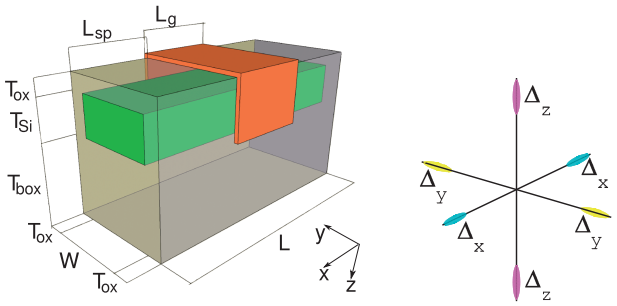

Fig. 1. On the left, the scheme of the simulated device is shown. Dark green represents the silicon nanowire. The tri-sided gate is highlighted in orange, whereas the source and drain contacts are in green and silicon dioxide is in gray. On the right, the six Δ valleys of bulk (001) silicon are reported, highlighting the three different valley couples with different colors: cyan, yellow, and magenta for valleys with the major axis along the k_x, k_y, and k_z directions, respectively.

$$\left[\mathbf{p}^{\mathrm{T}}\frac{\mathbf{M}_j}{2}\mathbf{p} + \frac{e}{2}(\mathbf{p}^{\mathrm{T}}\mathbf{M}_j\mathbf{A} + \mathbf{A}^{\mathrm{T}}\mathbf{M}_j\mathbf{p}) + V + V_{\mathrm{xc}}\right]\Psi_{i,j,\sigma} = \varepsilon_{i,j,\sigma}\Psi_{i,j,\sigma} \quad (1)$$

where $\mathbf{p} = -i\hbar\nabla$ and $\mathbf{A} = \mathbf{A}_0 + \mathbf{A}_{\mathrm{xc}}$. $\mathbf{M}_j$ is the tensor of the inverse of the effective masses of the j-th pair of valley ($j = x, y, z$). $\mathbf{A}_0$ si the vector potential, and V is the scalar potential that includes Hartree and Zeeman terms. $\mathbf{A}_{\mathrm{xc}}$ and V_{xc} are the exchange–correlation vector and scalar potentials, which depend on the local spin-up and spin-down electron densities and on the local paramagnetic current density. $\varepsilon_{i,j,\sigma}$ and $\Psi_{i,j,\sigma}$ are the i-th eigenvalues and eigenfunctions, respectively, of the j-th pair of valley and spin σ ($\pm 1/2$). A valley splitting ΔE_{vo} between the pair of valleys along the k_y direction (Δ_y valleys) has been imposed to mimic the effect of the valley–orbit couplings.[20)] The same has been

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done for the valleys along the k_z direction (Δ_z valleys), whereas no valley splitting has been added between the couple of valleys along the k_x direction (Δ_x valleys) because no Si/SiO_2 interface along the x-axis is present (see Fig. 1). The final shape of the confining potential energy is reached by self-consistently solving the Poisson equation without assuming any particular shape of the tunnel barrier at the drain and source ends. The simulation ends when the error between the electrical potential in the last iteration and the previous one is under a given value. The many-body problem is solved in the entire silicon nanowire and in a 1-nm-thick region inside the surrounding oxide. Potentials to the tri-sided gate, source, and drain regions are applied, whereas a zero electric field z-component boundary condition is forced at the bottom of the device. We simulate the electrostatic behavior of different SETs at $T = 0.3\,\mathrm{K}$ at the drain voltage $V_d = 0\,\mathrm{V}$ with the gate voltage V_g chosen in order to align the N-th energy level of the quantum dot with the Fermi levels at the source and drain planes for each occupation number N, from 1 to 10. The conversion from the applied gate voltages to the corresponding addition energies E_{add} is obtained as

$$E_{add}(N) = \alpha(V_g(N+1) - V_g(N)), \tag{2}$$

where $V_g(N)$ and $V_g(N+1)$ are the gate voltages when N and $(N+1)$ electrons are present, respectively, and $\alpha = C_g/(C_g + C_s + C_d)$ is the lever-arm factor with C_g, C_s, and C_d as the gate, source, and drain capacitances, respectively. The valley filling has been investigated as a function of the number of electron N inside the quantum dot for different nominal sizes of the SET. We considered SETs with two gate lengths $L_g = 22$ and 25 nm and two gate widths $W =$ 10 and 15 nm. These values correspond to the limits of a $20 \times 20\,\mathrm{nm}^2$ nominal MOSSET within the tolerance of state-of-the-art lithographic process.[16] Moreover, SETs with $T_{Si} = 9$ and 10 nm have been studied. The energy splitting between the pair of Δ_y valleys, namely, $|\Delta E_{vo,y}|$, and that between the pair of Δ_z valleys, namely, $|\Delta E_{vo,z}|$, are considered separately, and they have been estimated by using eq. (25) reported by Friesen *et al.*,[21] which gives an approximated expression of the energy splitting between valleys of the same type in the case of a finite square well. The calculated values are reported in Table I. For each SET, the lever-arm factor α can be calculated by estimating the gate, source, and drain capacitances, and the resulting α parameters together with the geometrical sizes of the SETs are shown in Table I.

In Fig. 2 the electron density from $N = 1$ to 5 electrons is reported for SETs a, b, c, and d, respectively. Following the association color valley of Fig. 1 where cyan, yellow, and magenta colors represent the shells of Δ_x, Δ_y, and Δ_z valleys, respectively, the mixed color indicates which valleys are occupied by the electron(s). When $T_{Si} = 9\,\mathrm{nm}$ [Fig. 2(a)], the first two electrons fill the Δ_z valleys, and for higher N, the Δ_y valleys are also filled. This fact is due to the condition $W > T_{Si}$, and so the confinement is slightly stronger along the z-direction than along the y-axis. Conversely, for $T_{Si} = 10\,\mathrm{nm}$ [Fig. 2(b)], the first and second electrons occupy Δ_y valleys and then both Δ_y and Δ_z valleys are filled for $N = 3$ to 5. Small changes in T_{Si} modify strongly the filling sequence, suggesting that the T_{Si} has to be controlled carefully to maintain the same filling pattern. We performed similar simulations by changing the gate length L_g of the SET. In Figs. 2(b) and 2(c), the electron densities of SET b with $L_g = 25\,\mathrm{nm}$ and SET c with $L_g = 22\,\mathrm{nm}$ are compared. In these two cases, the filling sequence is the same for $N = 1$ to 4 with electrons that first occupy the Δ_y valleys and then the Δ_z ones, highlighting an irrespectiveness to 15% variation of the size of the system by maintaining the valley filling pattern. In Figs. 2(c) and 2(d), the electron densities of SET c with $W = 10\,\mathrm{nm}$ and SET d with $W = 15\,\mathrm{nm}$ are compared. The two filling sequences have different qualitative behaviors. In particular, in Fig. 2(c), Δ_y valleys are filled when $N = 1$ and 2, and then Δ_z valleys are also occupied for $N = 3$ to 5. In Fig. 2(d), only the eigenstates of Δ_z are filled. These results suggest that even for the first electrons, the valley filling sequence is dramatically sensitive to the variability of W in this kind of device. As the process variability on T_{Si} is normally much smaller than that on W, a design rule to make possible the filling of states belonging to the same couple of valleys — in particular, to Δ_z valleys — is to impose a gate width much larger than the silicon thickness $W \gg T_{Si}$ [see Fig. 2(d)]. For each device, adding electrons implies a greater spread of the charge density distribution along the x-axis due to the Coulomb repulsion among the electrons. Moreover, note that

Table I. Identifier, geometric sizes in nm, valley splitting energy in μeV in Δ_y and Δ_z valleys, and α parameter in eV/V for the different SETs.

SET	L_g	W	T_{Si}	$\lvert\Delta E_{vo,y}\rvert$	$\lvert\Delta E_{vo,z}\rvert$	α
a	25	10	9	190	272	0.8544
b	25	10	10	190	190	0.8485
c	22	10	10	190	190	0.8233
d	22	15	10	40	190	0.7715

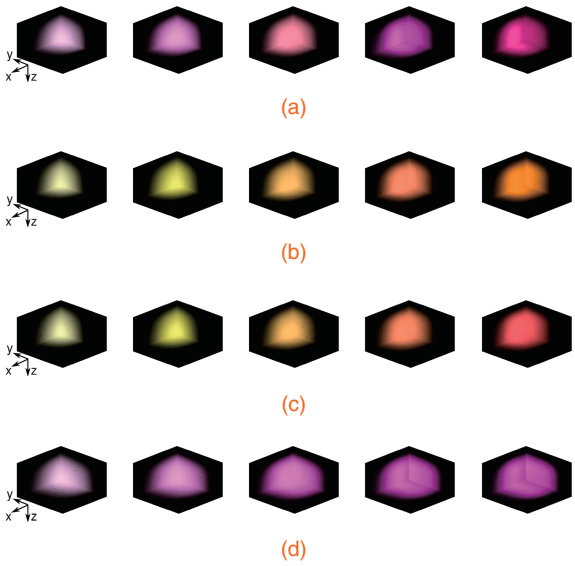

Fig. 2. Electron density for $N = 1$ to 5 electrons on the planes passing through the center of the wire for SETs a, b, c, and d, respectively. Pure cyan, yellow, and magenta colors represent the shells of Δ_x, Δ_y, and Δ_z valleys, respectively. Each added electron contributes to reinforcing the color of the valley filled. Only the case d in pure magenta consists of a quantum dot in which a single pair of valleys (Δ_z) is progressively filled up to 5 electrons. Cyan is not present as the Δ_x valleys are always empty.

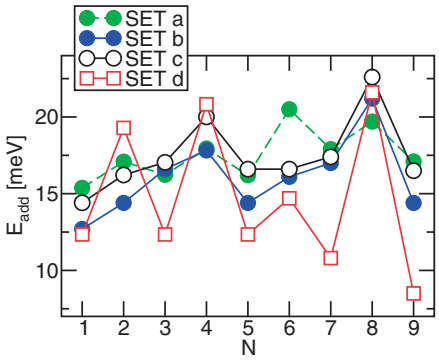

Fig. 3. Addition energies as a function of the number of electrons N for SETs a, b, c, and d.

in each SET, no electron fills the Δ_x eigenvalues, which have an energy higher than the other valleys due to their smaller effective mass along the y- and z-directions and due to the condition $L_g > T_{Si}, W$.

In Fig. 3, the addition energy E_{add} as a function of the number of electrons N is reported for the different SETs a, b, c, and d. SET a with $T_{Si} = 9$ nm presents high addition energies with small peaks for N even. Such high addition energies are due to the small gate capacitance, which implies a high charging energy. The addition energies of SET b with $L_g = 25$ nm are lower than those of the shorter SET c with $L_g = 22$ nm. The behavior is explained by considering that a reduction of L_g decreases the gate capacitance and consequently increases the charging energy, inducing an upshift of the addition energy patterns. Both SET b and c present a high addition energy peak for $N = 8$ when the added electron occupies a new shell from Δ_z valleys. SET d presents high addition energies for N even and small values for N odd, a sequence which recalls magic numbers observed for GaAs quantum dots in the past.[22] The sequence is related to the complete filling of shells from Δ_z valleys for $N = 2$ and 4 and also from Δ_y valleys for $N = 6$ and 8. Indeed, peaks in the addition energy pattern are present when an electron is added to a new shell.[17,23] All the reported results are obtained assuming that there are no extra sources of electric potential such as charged traps in the silicon and/or in the silicon dioxide, which would strongly affect the filling pattern of the energy levels and the corresponding charge distribution in the SET.

To conclude, according to our CS-DFT simulations, variations of W and T_{Si} of a nanowire SOI-MOSSET with squared sections entail important changes in the valley filling sequences, whereas the variability of L_g does not imply a significant modification of the filling patterns. The filling of states belonging only to Δ_z valleys is possible for the first electrons if the silicon thickness is much smaller than the width. Our results provide useful indications on the different criticalities of the fabrication parameters in order to create robust shell structures less sensitive to the process variability and suitable for a reliable qubit implementation.

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