Two-Dimensional Tunnel Transistors Based on Bi_2Se_3 Thin Film

Qin Zhang, *Member, IEEE*, Giuseppe Iannaccone, *Senior Member, IEEE*, and Gianluca Fiori, *Member, IEEE*

***Abstract*— A planar 2-D tunnel field-effect transistor based on Bi_2Se_3 thin film is proposed and simulated self-consistently via 2-D Poisson equation and a two-band transport model within the non-equilibrium Green's function formalism. A 2-quintuple layer Bi_2Se_3 thin film with a thickness of 1.4 nm and bandgap of 0.252 eV is used as channel material. We show that with high source/drain doping and drain underlap, the proposed device can work for ultralow power applications (supply voltage of 0.2 V), showing an ON/OFF current ratio of 10^4, and a dynamic power indicator 10 times lower than CMOS technology with comparable dimensions.**

***Index Terms*— Band-to-band tunneling (BTBT), transistor, subthreshold swing, NEGF, Bi_2Se_3.**

I. Introduction

TUNNEL field-effect transistors (TFETs) have been proposed as a promising technology in order to limit power dissipation, the main problem in integrated circuits nowadays [1]–[3]. It is the reduced subthreshold swing *SS* that enables TFETs to operate at low supply voltages, which however, requires a strong gate-channel coupling, generally achieved with high-k gate oxides, multiple-gate geometries, and thin body of the channel materials [1]–[3]. Since 2004 2-D materials [e.g. graphene [4] and Two-dimensional Metal Dichalcogenides (TMD)] have raised great interest within the device research community [5]. With 2-D materials, the transistor channel thickness can be scaled down to less than 1 nm, largerly improving the immunity to short channel effects [6]–[8]. However, neither the zero bandgap (E_G) graphene, nor the large bandgap (>1 eV) TMDs so far can be directly used in TFETs for logic applications: the former cannot be switched off, while the latter can hardly achieve the desired drive current. Graphene nanoribbons with tunable bandgap from 0.27 eV to $\sim$1 eV have been simulated and demonstrated with low subthreshold swing and promising performance [9]–[12]. However, fabricating sub-5-nm nanoribbons without width variation and edge roughness still remains a big challenge. Recently, the availability of ultra-thin topological insulators with bandgap of 0.14 eV $\sim$ 0.5 eV [13], [14] has opened new opportunities for planar 2-D TFET design [15]. Bi_2Se_3, a topological insulator, has a rhombohedral crystal structure with Se1–Bi1–Se2–Bi1'–Se1' five atoms as one unit cell, also called one quintuple layer (1-QL) [16] (Fig. 1(a)). As a difference from the bulk material thin films of Bi_2Se_3 with less than 6 QLs have shown bandgaps from 41 meV to $\sim$0.5 eV [13].

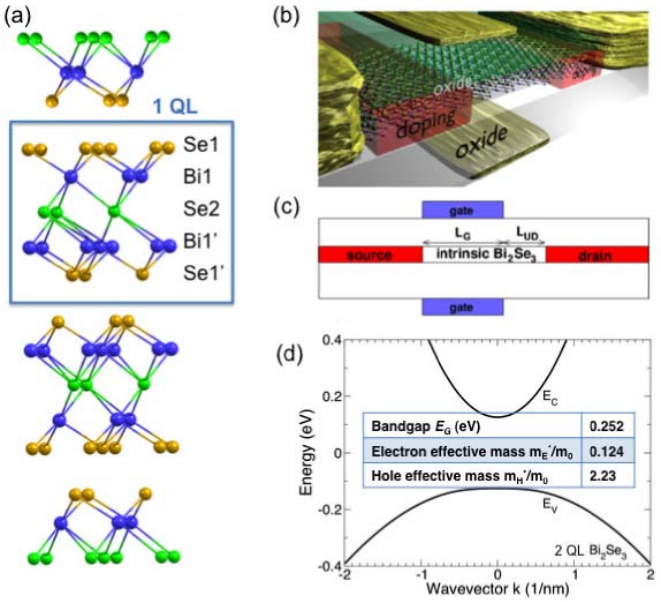

Fig. 1. (a) Crystal structure of Bi_2Se_3 with Se1–Bi1–Se2–Bi1'–Se1' five atoms as a quintuple layer (QL). (b) Schematic of the simulated double-gate Bi_2Se_3 TFET. (c) Longitudinal cross-section of the simulated device. The gate length is L_G, the drain underlap is L_{UD}, and the oxide is 1.1 nm HfO_2. (d) Band structure of 2 QL Bi_2Se_3. The inset table shows the band gap and the effective masses of electrons and holes extracted at $k = 0$.

In this letter, we focus on the 2QL Bi_2Se_3 with a bandgap of 0.252 eV and explore the potential of this ultra-thin Bi_2Se_3 based TFETs for low power logic application through atomistic quantum simulations. It is shown that an ON/OFF current ratio of 4 orders of magnitude is achievable with a supply voltage (V_{DD}) of 0.2 V.

II. Simulation Approach

The simulated n-type planar double-gate TFET structure is depicted in Fig. 1(b) and (c), where the 2QL Bi_2Se_3 is used as the active channel material, with a thickness of 1.4 nm and a relative static dielectric constant ε_r of 100 (from bulk Bi_2Se_3 [17]). The oxide is 1.1 nm HfO_2 with $\varepsilon_r = 25$. The source is heavily doped (p^+) with a degeneracy of ΔE_S, and the drain is n^+ with a degeneracy of ΔE_D (Fig. 2(a)). In experiments, high doping concentrations can be realized electrostatically or chemically [18]. Different gate lengths

Manuscript received October 3, 2013; revised October 23, 2013; accepted October 24, 2013. Date of publication November 20, 2013; date of current version December 20, 2013. This work was supported in part by the EC FP7 Project GRADE under Contract 317839 and in part by the EC FP7 Project STEEPER under Contract 256267. The review of this letter was arranged by Editor E. A. Gutiérrez-D.

The authors are with the Department of Information Engineering and SEED-PUSL, University of Pisa, Pisa 56122, Italy (e-mail: quin.zhang@for.unipi.it).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2013.2288036

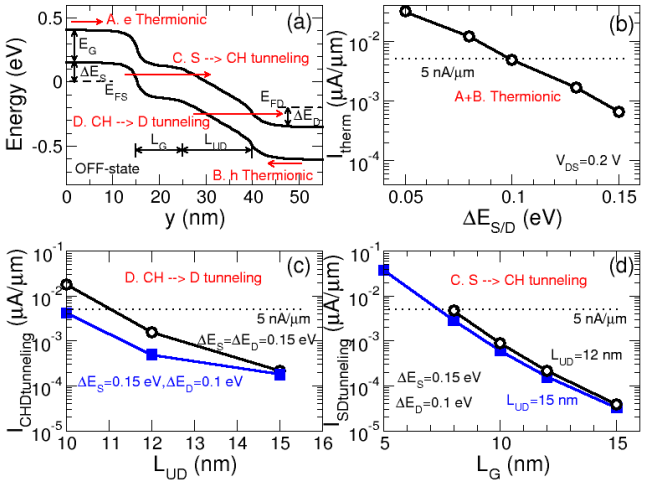

Fig. 2. (a) OFF-state band diagram of the Bi_2Se_3 TFET at $V_{DS} = 0.2$ V, showing four possible current leakages: A. electron thermionic current, B. the hole thermionic current, C. the source-to-channel tunneling, and D. the channel-to-drain tunneling. E_{FS} and E_{FD} are the Fermi levels in the source and drain respectively. (b) The thermionic current as a function of the source/drain degeneracy. (c) The channel-to-drain tunneling current as a function of the drain underlap with $L_G = 10$ nm and different doping degeneracies. (d) The source-to-channel tunneling current as a function of the gate length with $\Delta E_S = 0.15$ eV, $\Delta E_D = 0.1$ eV, and $L_{UD} = 12$ or 15 nm.

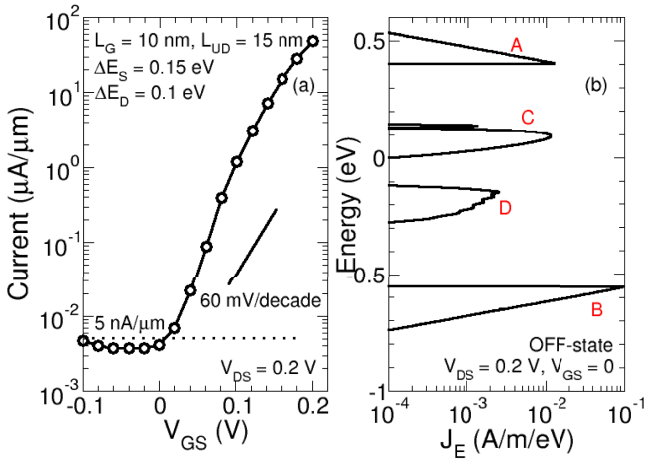

Fig. 3. (a) Transfer characteristic of the n-type 2QL Bi_2Se_3 TFET at $V_{DS} = 0.2$ V and room temperature. The effective subthreshold swing over 4 orders of magnitude is 50 mV/decade. (b) The current spectrum in the OFF-state, showing all the four leakage components are well managed.

(L_G) and drain underlaps (L_{UD}) have been considered [10]. All the simulations are driven to assess the performance for ultra-low voltage applications, i.e., considering a supply voltage V_{DD} of 0.2 V.

The k.p Hamiltonian with periodic boundary condition in the transverse direction is represented in the real space. The parameters are extracted from [19] to fit the conduction and valence bands measured through angle-resolved photoemission spectroscopy (ARPES) [13]. Figure 1(d) shows the band structure of 2QL Bi_2Se_3 from [13], where the band gap is 0.252 eV, comparable to that of a 5 nm graphene nanoribbon [11]. Ballistic transport is solved self-consistently with the 2D Poisson equation, within the Non-Equilibrium Green's function (NEGF) formalism, exploiting the NanoTCAD ViDES simulation environment [20], [21].

III. Results and Discussion

For ultra-low power logic applications, it is important to understand the OFF-state leakage current and maintain it as low as 5 nA/μm [22]. In Fig. 2(a), we show a sketch of the band diagram in the OFF-state and the main contributions to the OFF-state current (I_{OFF}). There are four important components: A) electron thermionic emission, B) hole thermionic emission, C) source-to-channel tunneling from source valence band edge to the channel conduction band edge, and D) channel-to-drain tunneling from channel valence band edge to the drain conduction band edge. To obtain a low I_{OFF}, the device has to be properly designed as to maintain all the four components low.

First, for narrow bandgap materials, thermionic current (A + B) can greatly affect the I_{OFF}, which has to be reduced by high doping level in both source and drain. As shown in Fig. 2(b), the degeneracy for both source and drain, ΔE_S and ΔE_D, has to be at least 0.1 eV to keep the thermionic current component lower than 5 nA/μm.

However, the large degeneracy makes the total tunneling energy window ($\Delta E_S + \Delta E_D + qV_{DS} \geq 0.4$ eV) larger than the bandgap (0.252 eV) in the channel, Fig. 2(a), so that the channel-to-drain tunneling (D) cannot be simply blocked by the bandgap as seen in TFETs with large bandgap materials [1], [2]. In order to improve transistor performance in the OFF-state, we introduce a drain underlap [10], [23]. Fig. 2(c) shows the channel-to-drain tunneling current as a function of the drain underlap length L_{UD} for different doping (e.g. different carrier degeneracy). Even though higher degeneracy yields lower thermionic current as seen in Fig. 2(c), it also requires longer drain underlap to suppress the channel-to-drain tunneling, which in turn limits device scalability.

The gate length scaling is also limited by the source-to-channel tunneling. In Fig. 2(d), as the gate length L_G is scaled below 15 nm, the source-to-channel tunneling (C) increases exponentially, and reaches 5 nA/μm as L_G shrinks to about 8 nm. The drain underlap can help reducing the source-to-channel tunneling as well to some extent, by increasing the effective channel length.

Considering all components of the OFF-state leakage current, a TFET with $L_G = 10$ nm, $L_{UD} = 15$ nm, $\Delta E_{S/D} =$ 0.15/0.1 eV is designed and simulated. The transfer characteristic is shown in Fig. 3(a), where the OFF-state current is well managed to be 5 nA/μm, and an ON/OFF current ratio of 10^4 is achieved with a supply voltage of 0.2 V, indicating an effective subthreshold swing of 50 mV/decade. Fig. 3(b) plots the leakage current spectrum, the I_{OFF} distribution (J_E) with energy, showing all the four leakage components in details. The asymmetric doping of source and drain (larger ΔE_S) is designed considering both the drive current and the scaling of the device. Comparison of the proposed TFET to the 2018 low-power MOSFET target identified by the International Technology Roadmap for Semiconductors (ITRS) [22] is given in Table I, where C is the total gate capacitance including fringe capacitances. For the TFET, the total capacitance is

TABLE I
COMPARISON OF 2018 LOW-POWER MOSFET TARGET FROM ITRS ROADMAP [22], THIN BODY DOUBLE-GATE InAs TFET [3] AND THE PROPOSED 2 QL Bi_2Se_3 TFET

	2018 LP Multi-gate MOSFET [19]	Thin-body InAs TFET [3]	2QL Bi_2Se_3 TFET (this work)	unit
L_G (+L_{UD}): physical channel length	13.1	15	10 (+15)	nm
V_{DD}: power supply voltage	0.57	0.3	0.2	V
$I_{D,SAT}$: nMOS saturation current	794	15	48	μA/μm
SS: Effective subthreshold swing	> 60	86	50	mV/ decade
CV^2: nMOS dynamic power indicator	0.18	-	0.018	fJ/μm
$\tau = CV/I$: nMOS intrinsic delay	0.4	-	1.84	ps

calculated by charge difference in the ON- and OFF-state divided by V_{DD}. It is shown that the intrinsic switching speed of the Bi_2Se_3 TFET is 3.5X slower than that of the MOSFET, but its dynamic power indicator is as low as 1/10 of the MOSFET. Simulation results of a state-of-art thin body double-gate InAs TFET [3] are also shown in the table as a reference, where the effective suthreshold swing for TFETs is calculated by $V_{DD}/\log(I_{D,SAT}/I_{OFF})$. As can be seen, the atomic thin body of the proposed Bi_2Se_3 TFET improves the effective subthreshold swing and the drive current.

It has been noted that the high static dielectric constant ($\varepsilon_r = 100$) of Bi_2Se_3 is not favorable for short-channel field-effect transistors (FETs), due to the penetration of the lateral electric field into the channel [24]. For TFETs, this field penetration leads to a broadening of the source-channel junction, which reduces the source carrier injection efficiency in the ON-state and the drive current, so the effective subthreshold swing is degraded. From our simulation, the ON-state current can increase more than twice if one considers a channel material with $\varepsilon_r = 20$. The reduction of the field penetration could also reduce the fringe capacitance and enhance the speed. It is worth mentioning that, as far as we are aware, there are no reported measurements of the static dielectric constant of ultra-thin Bi_2Se_3, which might be different from the bulk property we used in this letter.

IV. CONCLUSION

The Bi_2Se_3 thin film with bandgap of 0.252 eV is proposed as TFET channel material for low-power logic applications. With high source/drain doping and a drain underlap, the 2-D Bi_2Se_3 TFET can operate with a supply voltage of 0.2 V with $I_{OFF} = 5$ nA/μm and ON/OFF current ratio $= 10^4$. The ON current is low compared to CMOS technology, and is responsible for the larger intrinsic delay of the proposed TFET. However, the very small supply voltage enables a very competitive dynamic power indicator, 10 times lower than CMOS, which makes the device promising for very low-power applications.

REFERENCES

[1] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[2] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," *Nature*, vol. 479, pp. 329–337, Nov. 2011.

[3] U. E. Avci, S. Hasan, D. E. Nikonov, *et al.*, "Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results," in *Proc. Symp. VLSI Technol.*, 2012, pp. 183–184.

[4] K. S. Novoselov, A. K. Geim, S. V. Morozov, *et al.*, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, pp. 666–669, Oct. 2004.

[5] S. Z. Butler, S. M. Hollen, L. Cao, *et al.*, "Progress, challenges, and opportunities in two-dimensional materials beyond graphene," *ACS Nano*, vol. 7, no. 4, pp. 2892–2926, Apr. 2013.

[6] D. Jena, "Tunneling transistors based on graphene and 2-D crystals," *Proc. IEEE*, vol. 101, no. 7, pp. 1585–1602, Jul. 2013.

[7] B. Radisavljevic, A. Radenovic, J. Brivio, *et al.*, "Single-layer MoS_2 transistors," *Nature Nanotechnol.*, vol. 6, no. 3, pp. 147–150, Mar. 2011.

[8] G. Fiori and G. Iannaccone, "Ultralow-voltage bilayer graphene tunnel FET," *IEEE Electron Device Lett.*, vol. 30, no. 10, pp. 1096–1098, Oct. 2009.

[9] Q. Zhang, T. Fang, H. L. Xing, *et al.*, "Graphene nanoribbon tunnel transistors," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1344–1346, Dec. 2008.

[10] P. Zhao, J. Chauhan, and J. Guo, "Computational study of tunneling transistor based on graphene nanoribbon," *Nano Lett.*, vol. 9, no. 2, pp. 684–688, Feb. 2009.

[11] M. Luisier and G. Klimeck, "Performanceanalysis of statistical samples of graphene nanoribbon tunneling transistors with line edge roughness," *Appl. Phys. Lett.*, vol. 94, pp. 223505-1–223505-3, Jun. 2009.

[12] S. K. Chin, D. Seah, K. T. Lam, *et al.*, "Device physics and characteristics of graphene nanoribbon tunneling FETs," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 3144–3152, Nov. 2010.

[13] Y. Zhang, K. He, C.-Z. Chang, *et al.*, "Crossover of the three-dimensional topological insulator Bi_2Se_3 to the two-dimensional limit," *Nature Phys.*, vol. 6, pp. 584–588, Aug. 2010.

[14] L. He, X. F. Kou, and K. L. Wang, "Review of 3D topological insulator thin-film growth by molecular beam epitaxy and potential applications," *Phys. Status Solidi, Rapid Res. Lett.*, vol. 7, pp. 50–63, Feb. 2013.

[15] J. Chang, L. F. Register, and S. K. Banerjee, "Possible applications of topological insulator thin films for tunnel FETs," in *Proc. Device Res. Conf.*, 2012, pp. 31–32.

[16] H. Zhang, C.-X. Liu, X.-L. Qi, *et al.*, "Topological insulators in Bi_2Se_3, Bi_2Te_3 and Sb_2Te_3 with a single Dirac cone on the surface," *Nature Phys.*, vol. 5, pp. 438–442, Jun. 2009.

[17] H. Kohler and C. R. Becker, "Optically active lattice vibrations in Bi_2Se_3," *Phys. Stat. Solidi B*, vol. 61, pp. 533–537, 1974.

[18] D. Kim, S. Cho, N. P. Butch, *et al.*, "Surface conduction of topological Dirac electrons in bulk insulating Bi_2Se_3," *Nature Phys.*, vol. 8, no. 6, pp. 459–463, Jun. 2012.

[19] H.-Z. Lu, W.-Y. Shan, W. Yao, *et al.*, "Massive Dirac fermions and spin physics in an ultrathin film of topological insulator," *Phys. Rev. B*, vol. 81, pp. 115407-1–115407-7, Mar. 2010.

[20] G. Fiori and G. Iannaccone, "Multiscale modeling for graphene-based nanoscale transistors," *Proc. IEEE*, vol. 101, no. 7, pp. 1653–1669, Jul. 2013.

[21] G. Fiori and G. Iannaccone. (2013, Oct. 30). *NanoTCAD ViDES* [Online]. Available: http://vides.nanotcad.com

[22] Process Integration, Devices, and Structures (PIDS), Taiwan. (2012). *International Technology Roadmap for Semiconductors (ITRS)* [Online]. Available: http://www.itrs.net/Links/2012ITRS/Home2012.htm

[23] G. Giusi and G. Iannaccone, "Junction engineering of 1T-DRAMs," *Electron Device Lett.*, vol. 32, no. 3, pp. 408–410, Mar. 2013.

[24] J. Chang, L. F. Register, and S. K. Banerjee, "Topological insulator Bi_2Se_3 thin films as an alternative channel material in metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 112, no. 12, pp. 124511-1–124511-6, Dec. 2012.