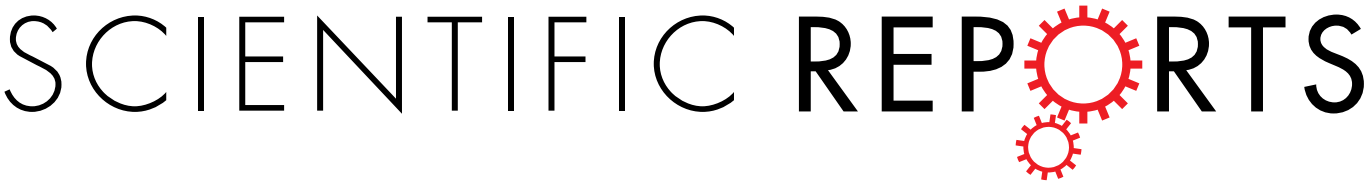

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Material-Device-Circuit Co-optimization of 2D Material based FETs for Ultra-Scaled Technology Nodes

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Two-dimensional (2D) material based FETs are being considered for future technology nodes and high performance logic applications. However, a comprehensive assessment of 2D material based FETs has been lacking for high performance logic applications considering appropriate system level figure-of-merits (FOMs) e.g. delay, and energy-delay product. In this paper, we present guidelines for 2D material based FETs to meet sub-10 nm high performance logic requirements focusing on material requirement, device design, energy-delay optimization for the first time. We show the need for 2D materials with smaller effective mass in the transport direction and anisotropicity to meet the performance requirement for future technology nodes. We present novel device designs with one such 2D material (monolayer black-phosphorus) to keep Moore's alive for the HP logic in sub-5 nm gate length regime. With these device proposals we show that below 5 nm gate lengths 2D electrostatistics arising from gate stack design becomes more of a challenge than direct source-to-drain tunneling for 2D material-based FETs. Therefore, it is challenging to meet both delay and energy-delay requirement in sub-5 nm gate length regime without scaling both supply voltage (V_{DD}) and effective-oxide-thickness (EOT) below 0.5 V and 0.5 nm respectively.

To keep Moore's law alive, silicon based tri-gate FinFETs are being used for high performance logic at current technology nodes. With each technology generation, these devices achieve 15% boost in ON current, 50% reduction in energy-delay product, and 0.5x area scaling[1,2]. To further continue this trend, alternative channel materials e.g. SiGe, Ge, III-V, and novel device architectures e.g. gate-all-around nanowire (NW) FETs are being explored for future technology nodes. III-V materials due to its lower effective mass and electron-phonon scattering promise higher mobilities, thus higher ON currents for logic applications. But, the lower effective mass also poses challenges such as losing control on electrostatistics with the scaling of channel length, and lower charge concentrations owing to limited density-of-states (DOS)[3]. Device architectures such as gate-all-around (GAA) FETs promise to achieve better electrostatistics at scaled gate lengths.

Alternatively, 2D materials are considered for high performance logic roadmap due to their atomic thickness, which offer better scalability in comparison to Si and III–V channel FETs[4]. Within the 2D materials family, monolayer black phosphorus based FET has recently gained popularity as a promising high-performance (HP) logic device option at the end of the semiconductor roadmap due to its superior transport properties[5]. Monolayer (ML) BP shows anisotropic properties such as lower effective mass in armchair direction and 8x higher effective mass in zigzag direction. By aligning the ML BP channel length in armchair direction and channel width in zigzag direction we can achieve higher carrier velocity (mobility) and higher density-of-states (i.e. inversion charge density) respectively, which can effectively result in higher on-state currents. With full-band dissipative simulations, currents in monolayer black phosphorus (ML BP) FETs are reported to be significantly higher than other ML TMD based FETs[6,7]. The dissipative current in ML BP FET is shown to be around 90% of the ballistic current for 10 nm gate length. Having said that, the lower effective mass in the transport direction pose challenges in maintaining good sub-threshold slope below 10 nm gate lengths in ML BP FET in comparison to other TMD based FETs. Moreover, the efforts to have the stable BP under ambient condition are ongoing[8,9]. Nevertheless, to

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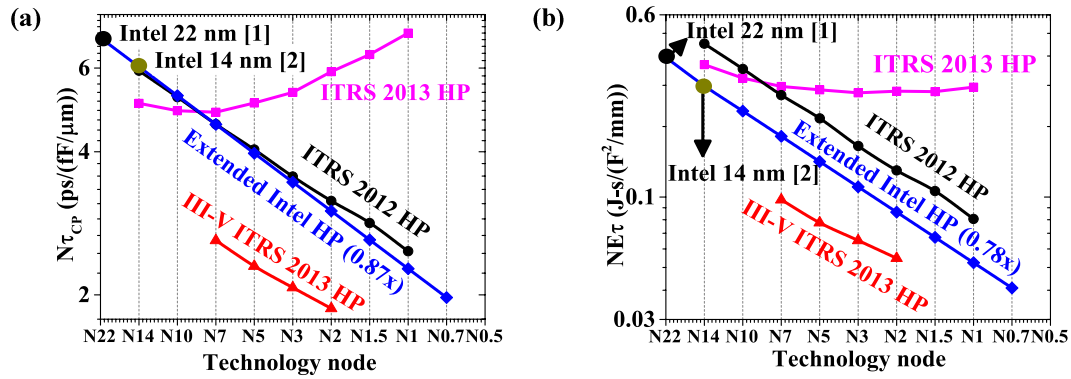

Figure 1. High-performance logic roadmap, (**a**) Normalized delay ($N\tau_{CP}$) and, (**b**) Normalized energy-delay product ($NE\tau$) with technology nodes for $\alpha = 0.1$, and $L_D = 10$ (HP logic).

evaluate real potential of such materials for high performance logic in sub-10 nm technology nodes, we need to co-optimize material and different device designs to achieve the required circuit-level metrics such as delay, and energy-delay product.

In this paper, using quantum transport simulations of monolayer 2D materials-based-FETs, we analyze the cause of such performance degradation in sub-10 nm gate length regime due to both material and device parameters. We propose device structures with ML BP to enable scaling of gate length in sub-5 nm regime. Further, for a given technology node, we show the selection of supply voltage (V_{DD}) to achieve the required delay and an optimum energy-delay product (EDP).

Results and Discussion

Circuit-Level Requirements. In order to benchmark the 2D FETs at the circuit level and understand the energy-delay tradeoff, we choose delay and energy per operation as circuit level figure-of-merits (FOMs). We estimate these circuit level metrics for a simplified version of critical path in CMOS logic, with a CMOS inverter chain and balanced 2D FETs for both p- and n-type transistors. The first-order equations for delay and energy per operation can be written as ref. 10:

$$\tau_{CP} = \frac{C_{node}V_{DD}}{I_{ON}} \cdot L_D; \quad E_{tot} = C_{tot}V_{DD}^2(\alpha + L_D\frac{I_{OFF}}{I_{ON}}) \tag{1}$$

where τ_{CP} is the delay of the critical path with a logic depth L_D and the total capacitance of each node C_{node}. Total energy (E_{tot}) per operation can be written as sum of dynamic and leakage energy. Here, α, and C_{tot} denote the activity factor and the total capacitance of the logic design respectively.

Further, we normalize the total energy and delay by the capacitance of the chip, which is reasonable for the sub-10 nm technology nodes, when the total capacitance is dominated by interconnect capacitances instead of intrinsic device capacitance, given as:

$$N\tau_{CP} = \frac{V_{DD}}{I_{ON}} \cdot L_D; \quad NE_{tot} = V_{DD}^2(\alpha + L_D\frac{I_{OFF}}{I_{ON}}); \quad NE\tau = E_{tot} \cdot \tau_{CP} \tag{2}$$

here $N\tau_{CP}$, and NE_{tot} denote the normalized delay and total energy per operation respectively, while the energy-delay product ($NE\tau$) signifies that energy and speed are equally weighed for an optimized logic design.

As shown in Fig. 1, we extend the circuit-level high performance logic roadmap for sub-5 nm technology nodes by extrapolating scaling of normalized delay and energy-delay product from Intel 22 nm[1] to Intel 14 nm technology nodes[2] with reported 15% boost in ON current (for same supply voltage) and required 50% reduction in the energy-delay product. Thus, the scaling of normalized delay by 0.87x and normalized energy-delay product by 0.78x results in total capacitance scaling of around 0.8x with each technology node. Figure 1 shows that extended Intel HP requirements seems most reasonable in comparison to ITRS HP requirements while III-V ITRS HP requirements are quite ambitious.

Technology Requirements. To achieve area scaling of 0.5x with each technology node, the technology parameters such as contacted gate pitch (C_{GP}) and metal pitch (MP) are scaled by 0.7x with each technology generation. To scale C_{GP}, gate length (L_G) scaling has been the primary driver for past technology generations. But, due to process constraints, scaling of C_{GP} below 25 nm is not forseen[11]. Therefore, for future technology nodes it is imperative to scale gate lengths in sub-10 nm to relax constraints on spacer thickness and contact openings. Alternatively, technology options such as monolithic 3D integration are sought to further scale the area per function[12]. The technology parameters listed in Table 1 (till N2) are taken from III-V ITRS HP roadmap[13].

Device-Level Figure-of-Merits. We consider a double-gate monolayer 2D material based FET as shown in Fig. 2a. The electrical characteristics of 2D material based FETs are calculated using the framework described in methods section. The effect of different transport effective mass and channel lengths on ON current (I_{ON}) is

	N7	N5	N3	N2	N1.5	N1	N0.7
C_{GP} (nm)	42	32	25	?	?	?	?
L_G (nm)	11.7	9.3	7.4	5.8	4.5	3.5	2.7
V_{DD} (V)	0.61	0.58	0.56	0.54	?	?	?
EOT (nm)	0.62	0.56	0.5	0.45	?	?	?
I_{OFF} (A/m)	0.1	0.1	0.1	0.1	0.1	0.1	0.1

Table 1. III–V ITRS 2013 HP Roadmap extended for gate lengths below 5 nm. Supply voltage is denoted by V_{DD}. EOT denotes effective-oxide-thickness. Here, OFF current target (I_{OFF}) for HP logic is chosen to be 100 nA/μm.

shown in Fig. 2b. We can clearly see that a smaller effective mass 2D material is the preferred choice for high performance logic. Smaller transport mass 2D materials with anisotropic properties can offer higher carrier injection velocity and higher inversion charge density, resulting in higher on-state current provided we can maintain good electrostatistics with gate length scaling. To get physical insights in electrostatics of shorter gate length devices, we study the effect of transport effective mass on sub-threshold slope (S.S.) behavior for different gate lengths as shown in Fig. 2c. We break-down Fig. 2c into two regions: 1) At lower effective masses S.S. degrades due to direct S/D tunneling (due to material property); 2) At higher effective masses where the increase in S.S. with downscaling of gate lengths is attributed to 2D electrostatics.

Circuit-Level Figure-of-Merits. Figure 3 shows the combined effect of sub-threshold and super-threshold behavior on delay and energy-delay product for a given I_{OFF} of 100 nA/μm. We observe that till N3, 2D materials with smaller transport effective mass outperform the 2D materials with higher ones. It can be also seen that monolayer BP ($m_x^* = 0.15\, m_0$, $m_y^* = 1.2\, m_0$) FET can meet both extended Intel HP and III-V ITRS 2013 HP delay and energy-delay requirements for N7, and N5.

Proposed Device Structures. To further enable the HP logic roadmap with ML BP FETs, we need to improve electrostatistics for sub-10 nm channel lengths with novel device designs. We propose device designs which address improving both 2D electrostatistics and direct source-to-drain (S/D) tunneling.

Improving 2-D Electrostatistics. We introduce a low-k interfacial layer (IL) between ML BP and High-k dielectric to reduce fringing fields due to the gate stack at shorter gate lengths[14]. As shown in Fig. 4a, by reducing fringing fields we improve both the gate control (i.e. slope of gate capacitance with gate voltage) and effective gate capacitance in ON state. Further, Fig. 4b shows that the performance of ML BP FETs at $L_G = 7.4$ nm improves by more than 50% for the same effective-oxide-thickness (EOT) and physical thickness of the gate oxide (T_{OX}). For effective-oxide-thicknesses above 0.5 nm, we consider low-κ IL (SiO_2) to be between 0.4–0.6 nm and High-κ dielectric (HfO_2, ZrO_2, La_2O_3) to be 1–1.5 nm thick. To meet both extended Intel HP and III-V ITRS 2013 HP delay requirement with the device structure having low-k IL, we can relax EOT requirements of the N3 technology node. Further, to see prospects of such gate stack with gate length scaling, we consider equivalent direct S/D tunneling probability i.e. $\sim\exp(-L_G \cdot \sqrt{m_x^*})$ as shown in Fig. 4c. It shows that to achieve reasonable 2D electrostatistics below 4.5 nm gate length, we require EOT scaling below 0.5 nm irrespective of the direct S/D tunneling.

Reducing Direct Source-to-Drain Tunneling. We consider different device concepts (as shown in Fig. 5a) which employ depletion at the source/drain extension-to-channel junction in OFF state, resulting in larger tunneling lengths by modifying the potential profile at the junctions. Although, underlap (UL) and junctionless (JL) 2D material based FETs have been shown to improve direct source-to-drain tunneling at scaled gate lengths[15], such designs alone can't provide required performance below 5 nm gate lengths as shown in Fig. 5b. To achieve the required performance for sub-5 nm gate lengths, we propose extended back-gate device architecture in conjunction with UL/JL FET, which makes it possible to meet the performance requirements till N0.7 ($L_G = 2.7$ nm) for a fixed V_{DD}, and EOT. It is important to note that due to back-gate overlap in the extended back-gate architecture, an extra parasitic capacitance component as gate overlap capacitance comes in picture which may affect the total capacitance scaling, thus delay and energy-delay scaling. Nevertheless, Fig. 5c shows the need to scale V_{DD} to meet energy-delay requirement although the performance (delay) requirement is met till N0.7 for a fixed V_{DD}.

Energy-Delay Optimization. As shown in Fig. 6a, it is very challenging to meet both energy-delay and delay requirement even for smaller supply voltages for N1.5 and beyond. On the other hand, we see that the EOT requirement for N1.5 can be relaxed as shown in Fig. 6b, while Fig. 6c shows that we need to scale EOT below 0.5 nm to meet N1 requirements which scales the supply voltage. As EOTs below 0.5 nm become challenging to achieve using High-k dielectric with IL layer; it requires the advent of two-dimensional oxides with higher dielectric constant, and higher tunneling barrier with ML BP.

Effect of contact resistance and scattering. Lastly, to understand the limit on different contact resistances and different ballitsic ratios, we first optimize the device structure consisting of High-κ with IL and extended back-gate with underlap for technology node N3. The device parameters are taken from Table 1 and the optimized L_{UN} comes out to be 1 nm. As shown in Fig. 7a, both I_{ON} and $N\tau_{CP}$ degrades by increasing contact resistance (R_C). We notice the upper limit of contact resistance to be 125 Ω-μm considering no scattering in the

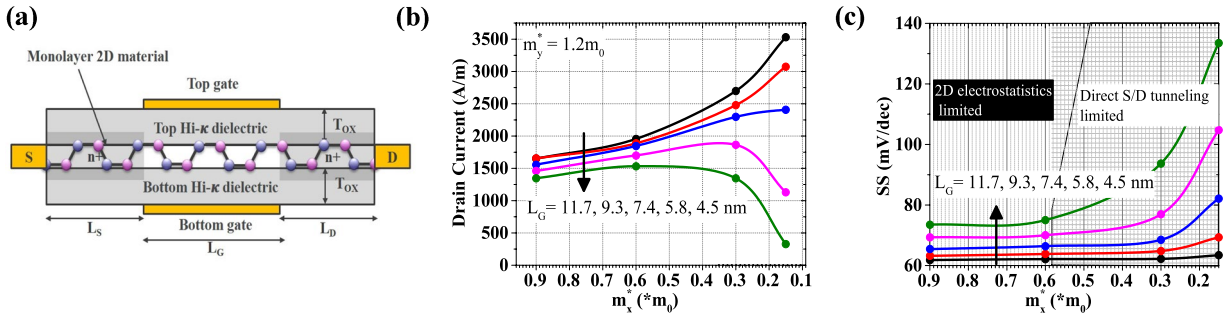

Figure 2. Device Simulations, (**a**) Double-gate monolayer 2D material based FET with $L_S = L_D = 15$ nm, and n^+ doping of source/drain $= 4 \times 10^{13}\, cm^{-2}$, and for a fixed transverse effective mass (m_y^*) effect of transport direction effective mass (m_x^*) and gate length (L_G) on, (**b**) ON current including effect of scattering and contact resistances, and, (**c**) Extracted subthreshold slope near OFF state.

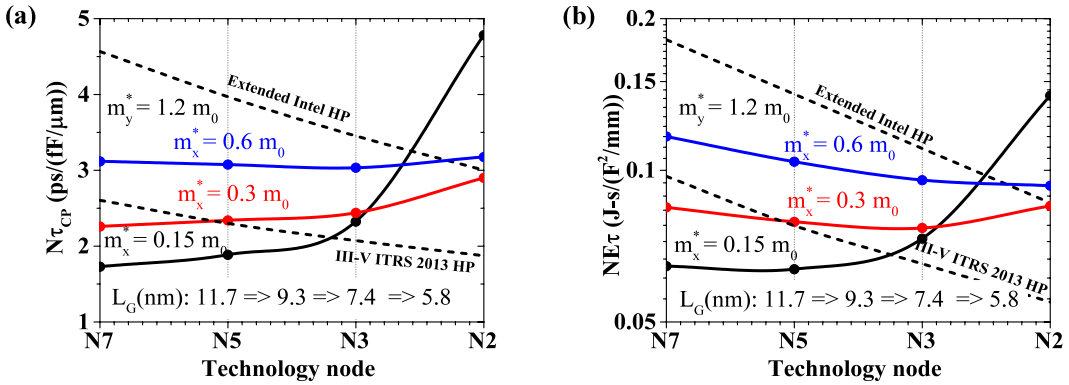

Figure 3. Performance of DG monolayer 2D FET at different technology nodes (**a**) Normalized delay and (**b**) Energy-delay product, showing the effect of gate length scaling of a smaller effective mass material such as monolayer black phosphorus (BP) ($m_x^* = 0.15\, m_0$, $m_y^* = 1.2\, m_0$) w.r.t. III–V ITRS 2013 HP and Extended Intel HP requirements.

channel. Further, Fig. 7b,c show that for R_C, ranging between 60 to 100 Ω-μm, we need to have ballisticity in the channel material between 85% to 60% respectively.

Conclusions

In this paper, we show that monolayer black phosphorus based FETs with different device designs can fulfill the high-performance logic energy-delay requirements till sub-5 nm gate lengths. Although the monolayer black phosphorus is reported to be unstable under ambient conditions and efforts to have the stable BP are ongoing, we infer that lower transport effective mass 2D material such as monolayer BP (with proposed device designs) perform better than higher effective mass 2D materials. To boost the performance of 2D material FET for advanced technology nodes, we propose device structures consisting of High-κ with IL (to increase the effective device gate capacitance), and extended back-gate with underlap (to curb direct source-to-drain tunneling). To meet the HP logic requirements, Table 2 lists the choice of device structure, and technology/device/circuit level parameters such as EOT/I_{ON}/V_{DD}. We see that for N1 and beyond, scaling of V_{DD} below 0.5 V becomes increasingly hard in order to meet both delay and energy-delay requirements, due to 60 mV/dec sub-threshold slope limit of FETs. It instigates the requirement of sleep sub-threshold slope transistors with effective ON currents ~2000 μA/μm.

Methods

The electrical characteristics of 2D material based FETs in the ballistic limit are calculated using a two-band tight binding (TB) Hamiltonian with a quantum transport simulation framework based on self-consistent solution of Poisson and Schrödinger equation with non-equilibrium Green's function within the NanoTCAD ViDES suite[16]. The two-band Hamiltonian for an anisotropic effective mass two-dimensional material with hexagonal lattice can be written as a 2×2 Hamiltonian matrix:

$$H_{2D} = \begin{bmatrix} E_{cm} & f(k) \\ f^*(k) & E_{vm} \end{bmatrix} \tag{3}$$

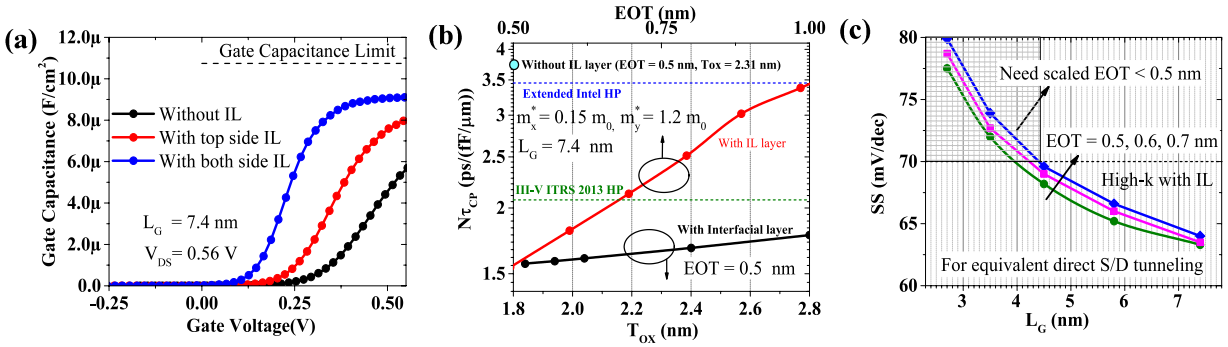

Figure 4. Effect of an interfacial layer (IL) with High-k dielectric, (**a**) On effective gate capacitance with gate voltage, (**b**) On performance (delay) of monolayer BP for N3 technology node i.e. $L_G = 7.4$ nm in two different cases (i) with different EOT, and (ii) with varying physical oxide thickness for same EOT, (**c**) On the scalability of such gate-stack for different EOT considering equivalent direct source/drain tunneling.

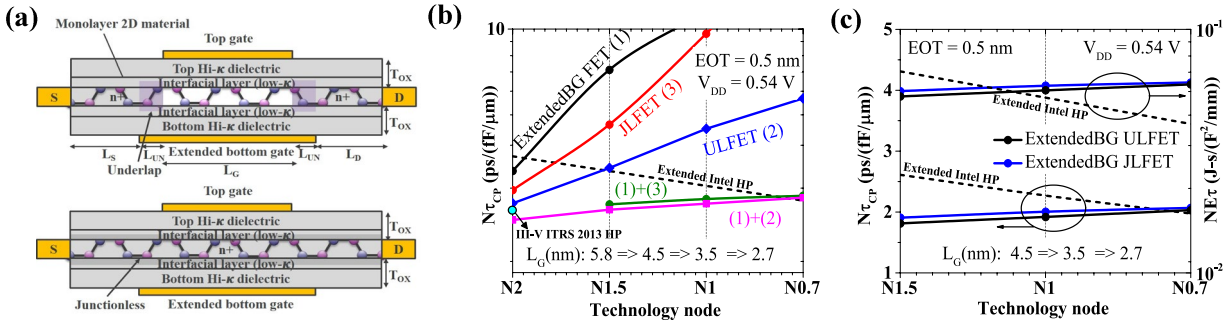

Figure 5. Reducing direct S/D tunneling for N2 and beyond (**a**) Device structures showing extended back-gate (BG) with underlap (ULFET) and extended BG with junctionless doping profile. (JLFET) (**b**) Effect of different combination of device structures on performance of monolayer BP FET for N2 and beyond for fixed EOT and supply voltage, showing the need of extended back-gate with UL/JLFET for $L_G = 4.5$ nm and beyond, (**c**) Delay and energy-delay product for extended BG UL/JFET ($L_{UN} = 2,3,4$ nm for N1.5, N1, and N0.7 respectively) showing that although we meet the performance requirement for N1 and N0.7, the energy-delay product doesn't scale.

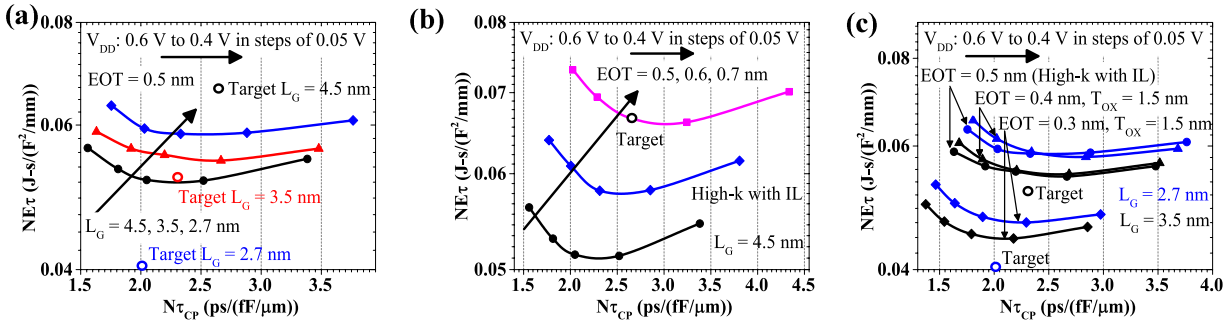

Figure 6. Supply voltage for optimum energy delay product, (**a**) Effect of supply voltage on energy and delay for fixed EOT = 0.5 nm, and $L_G = 3.5$, and 2.7 nm. (**b**) Effect of EOT scaling on energy-delay Vs delay plot for $L_G = 4.5$ nm, (**c**) For $L_G = 3.5$ nm, and $L_G = 2.7$ nm.

where E_{cm}, and E_{vm} denote the bottom of conduction band, and top of the valence band. Further, bandgap (E_G) of the material can be expressed as: $E_G = E_{cm} - E_{vm}$. Here, the $f(k)$ function, due to nearest neighbors, can be written as:

$$f(k) = t_1 e^{(-ik_x a/\sqrt{3})} + 2t_2 e^{(ik_x a/2\sqrt{3})} \cos\left(\frac{k_y a}{2}\right). \quad (4)$$

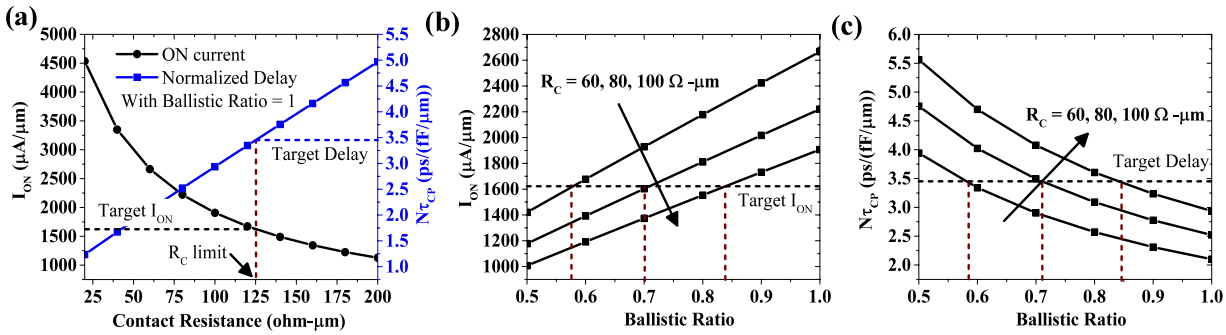

Figure 7. For N3 node with optimized device, (**a**) Effect of S/D contact resistance on ballistic ON current and delay, (**b**) Effect of ballistic ratio on ON current, (**c**) Delay, for different contact resistance values.

	N7	N5	N3	N2	N1.5	N1	N0.7
C_{GP} (nm)	42	32	25	?	?	?	?
L_G (nm)	11.7	9.3	7.4	5.8	4.5	3.5	2.7
V_{DD} (V)	0.61	0.58	0.56	0.54	0.5	0.47	0.45
EOT (nm)	>1	>1	~1	~0.8	~0.7	0.35	0.3
Device architecture	1	1	1	2	3	4	4
I_{ON} (A/m)	…	…	1657.5	1855.4	1939.7	2098	1961.5
I_{OFF} (A/m)	0.1	0.1	0.1	0.1	0.1	0.1	0.1

Table 2. Technology/device/circuit level parameters for high performance logic roadmap, and monolayer black phosphorus device architectures: (1) Double gate + High-k dielectric with IL, (2) Double gate + High-k dielectric with IL + Underlap, (3) Double gate + High-k dielectric with IL + extended BG + UL/JL, (4) Double gate + thinner 2D high-k oxide + extended BG + UL/JL. Here, ON current (I_{ON}) includes the effect of contact resistance and scattering.

Here, t_1, t_2 represents hopping energies in x and y direction respectively, which are calculated using the effective masses in x and y directions and bandgap of 2D material. k_x, and k_y are wave vectors in x & y directions, while a denotes the lattice constant of the two-dimensional hexagonal lattice. Further, using secular equation, we obtain the dispersion relation for the two-band model given as:

$$E^{\pm}(k) = \frac{(E_{cm} + E_{vm}) \pm \sqrt{(E_{cm} - E_{vm})^2 + 4\,|f(k)|^2}}{2}. \tag{5}$$

In order to calculate t_1 and t_2 for given effective masses in x and y direction, we use the parabolic effective mass approximation with the two-band model as:

$$\frac{1}{m_x^*} = \frac{1}{\hbar^2} \cdot \frac{\partial^2 E^{\pm}(k)}{\partial k_x^2} \quad \frac{1}{m_y^*} = \frac{1}{\hbar^2} \cdot \frac{\partial^2 E^{\pm}(k)}{\partial k_y^2} \tag{6}$$

where m_x^* and m_y^* denotes the reduced effective mass in x and y direction. Using Eqs 4–6, and by taking limit of the second derivative at the minimum energy k-point, we can calculate t_1 and t_2 for a given m_x^*, m_y^*, and E_G as:

$$|t_1|^2 = \frac{2\hbar^2 E_G}{3a^2 m_x^*} \quad |t_2|^2 = \frac{\hbar^2 E_G}{2a^2}\left[\frac{1}{3m_x^*} + \frac{1}{m_y^*}\right] \tag{7}$$

Further, to calculate practical currents from ballistic currents, first we calibrate our results with full-band dissipative simulations of ML BP FETs at 10.5 nm gate length using monolayer BP material parameters, which results in ballistic ratio of around 0.9 as mentioned in ref. 6. Moreover, the effect of source/drain contact resistances are included according to ITRS guidelines (i.e. linear degradation in the intrinsic ON current from 33% (in 2011) to 40% (in 2026)) to benchmark the performance of intrinsic 2D material based FETs with III-V ITRS HP roadmap[13]. Effectively, degradation of around 44% is considered in the ballistic currents due to scattering and contact resistance for Table 2.

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Author Contributions

T.K.A. performed the device simulations with contributions from G.F. in the definition of the anisotropic 2D material and benchmarked the devices with proposed figure-of-merits with contributions from W.D. B.S., I.R., P.R., G.I. and M.H. helped interpreting the simulation results. T.K.A. wrote the manuscript with contributions from all authors.

Additional Information

Competing Interests: The authors declare that they have no competing interests.

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