This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

A SPICE-Compatible Model of MOS-Type Graphene Nano-Ribbon Field-Effect Transistors Enabling Gate- and Circuit-Level Delay and Power Analysis under Process Variation

Ying-Yu Chen, *Student Member, IEEE,* Amit Sangai, Artem Rogachev, Morteza Gholipour, *Member, IEEE,* Giuseppe Iannaccone, *Fellow, IEEE,* Gianluca Fiori, and Deming Chen, *Senior Member, IEEE*

***Abstract*—This paper presents the *first* parameterized, SPICE-compatible compact model of a Graphene Nano-Ribbon Field-Effect Transistor (GNRFET) with doped reservoirs, also known as MOS-type GNRFET. The current and charge models closely match numerical TCAD simulations. In addition, process variation in transistor dimension, line edge roughness, and doping level in the reservoirs are accurately modeled. Our model provides a means to analyze delay and power of graphene-based circuits under process variation, and offers design and fabrication insights for graphene circuits in the future. We show that line edge roughness severely degrades the advantages of GNRFET circuits; however, GNRFET is still a good candidate for low-power applications.**

***Index Terms*—graphene, graphene nano-ribbon, GNRFET, transistor, SPICE, model**

I. Introduction

Field-effect transistors (FETs) built with carbon-based nano-materials have emerged as promising next-generation devices because of their outstanding electrical properties and integration capabilities via new fabrication techniques [1], [2], [3]. The most studied are carbon nanotube FETs (CNFETs) and graphene nano-ribbon FETs (GNRFETs). Compared to cylindrical carbon nanotubes (CNTs), graphene nanoribbons (GNRs) can be grown through a silicon-compatible, transfer-free, and *in situ* process [2], [4], [5], thus having no alignment and transfer-related issues as encountered by CNT-based circuits [2]. However, graphene-based circuits face other types of challenges, including small band gap, degraded mobility, and unstable conductivity due to process variation [6], [7], [8], [9], [10]. Therefore, it is important to evaluate these effects and provide a general assessment about the potential and usability of graphene circuits under realistic settings.

Since fabrication technology of GNRFETs is still in an early stage, transistor modeling has been playing an important role in evaluating futuristic graphene circuits. GNRFET simulations based on non-equilibrium Green's function (NEGF) formalism have been published [11], [12], which are the most accurate, but are also of the highest complexity. A semi-analytical model was developed in [13], but could not be straightforwardly used in circuit simulation since it still required non-closed-form numerical integrals. A lookup-table-based circuit-level simulator was implemented in [14], and an accurate physics-based compact model was developed in [15] using device-dependent curve-fitting. However, a major drawback of device-dependent models, either based on lookup tables or heavily-fitted equations, is that whenever the need to simulate a new device with a different design parameter arises, a complete set of device simulations are required to rebuild the model. This implies the infeasibility of using above models to perform design space exploration or evaluate the impact of process variation. In order to enable true exploration of graphene-based technology, a parameterized, SPICE-compatible model is required. This allows designers to input custom design parameters and quickly evaluate circuit functionality and performance. In our work, we developed our model based on a wide range of design parameters of sub-20-nm feature sizes, the scale in which GNRFETs are regarded as potential new devices. As a result, our model offers the same features as a typical compact model of a Si-CMOS transistor. Note that there has been research on modeling either CNFETs [16], [17] or Graphene FETs (GFETs[1][18]) in which such parameterized compact models are proposed, but we are the first to do so on GNRFETs. We have released this model on NanoHub [19] to aid designers in exploring graphene-based circuits and evaluating their potentials. For example, computer-aided design (CAD) algorithms targeting graphene-based circuits have been proposed [20], and they can definitely benefit from more accurate SPICE-level simulations.

In addition, most existing work regarding graphene circuits focuses either on logic gates [12], [14], [15] or on interconnects [3] without considering the entire system. We proposed a practical architecture that uses GNRs as both gates and local interconnects, and we discussed how GNRs and metal should be chosen as different interconnects to improve performance. We simulated digital circuits designed in this way by using our GNRFET SPICE model and compared their delay and power performance to that of the 16-nm Si-CMOS technology.

To summarize, the main contributions of our paper are as follows:

- Developing the first parameterizable SPICE-compatible GNRFET model.
- Modeling process variation in several design parameters as well as graphene-specific line edge roughness.

Y.-Y. Chen, A. Sangai, A. Rogachev, and D. Chen are with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL, USA. e-mail: chen150@illinois.edu.

M. Gholipour is with the Advanced VLSI Lab., School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran.

Giuseppe Iannaccone and Gianluca Fiori are with Dipartimento di Ingegneria dellInformazione, University of Pisa, Pisa, Italy.

Manuscript received XX, 2014; revised XX, 2014.

[1]A GFET is made of a zero-band-gap graphene sheet instead of GNRs, which are narrowed strips with finite band gaps. GFETs have a low I_{on}/I_{off} ratio and are more suitable in analog applications.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

- Proposing a GNR-based digital circuit architecture that integrates transistors and interconnects.
- Exploring the design space of GNRFET for desirable transistor-level properties.
- Analyzing transistor- and circuit-level properties of GNRFET circuits.
- Simulating non-trivial GNRFET circuits other than *inv* or ring oscillators, providing a realistic view on how GNRFET circuits perform.
- Comparing GNRFET circuits with Si-CMOS circuits.
- Performing Monte Carlo simulations on GNRFET circuits to provide insights on the effect of process variation.

The rest of the paper is organized as follows: Section II provides additional background on GNRFETs and discusses their use in logic gates; Section III presents our SPICE-compatible GNRFET model for the evaluation of GNRFET circuits; Section IV presents the experimental results; and Section V draws conclusions.

II. Building Circuits with GNRFETs

A. Graphene Properties and Fabrication Techniques

Graphene is a sheet of carbon atoms tightly packed into a two-dimensional honeycomb lattice. It is a zero-band-gap material, which makes it an excellent conductor by nature [2]. Graphene must be processed into narrow strips (GNRs) with widths below 10 nm in order to open a band gap and become semiconducting [2]. Theoretical work has shown that GNRs have band gaps inversely proportional to their widths [8]. Conductivity is also determined by the edge state [8]. GNRs with predominantly *armchair* edges are observed to be semiconducting, while GNRs with predominantly *zigzag* edges demonstrate metallic properties [2][2]. The width of a GNR (denoted W_{CH}) is commonly defined via the number of dimer lines N as illustrated in Figure 1, where $W_{CH} = (N-1)\cdot\sqrt{3}\times 0.144/2$ nm [22].

There are two varieties of GNRFETs: *SB-type* and *MOS-type* [2]. SB-type uses metal contacts and a graphene channel, which form Schottky barriers at junctions. In MOS-type GNRFETs, the reservoirs are doped with donors or acceptors. Doping with donors (acceptors) results in a N-type (P-type) GNRFET, in which current is dominated by electron (hole) conduction. MOS-type GNRFETs demonstrate a higher I_{on}/I_{off} ratio and outperform SB-type ones in digital circuit applications [12]. Therefore, we choose to model MOS-type GNRFETs here.

GNR fabrication techniques include lithography, chemical synthesis, and unzipping of carbon nanotubes [9], [23], [24], [25], [26], [27], etc. Due to limitation of resolution, lithography can only pattern GNRs down to 20 nm in width and tends to produce uneven edges [23]. In [24], a method to produce GNRs $\sim$ 4 nm was proposed, in which lithography is used to pattern GNRs and etching is used to narrow GNRs. Chemical synthesis can refine GNRs down to 2 nm in width [25].

[2]Although zigzag GNRs with pristine edges have a zero band gap, studies showed that band gap could actually be opened for zigzag GNRs with rough edges or those passivated with hydrogen atoms [10], [21]. In this work, we will focus on armchair GNRs.

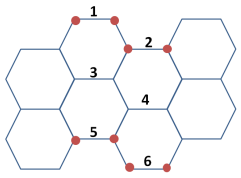


Fig. 1. Lattice structure of a armchair-type GNR with $N = 6$. N is the number of dimer lines in the armchair orientation.

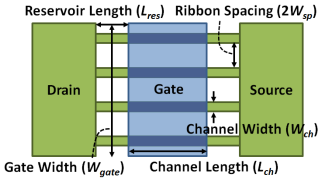


Fig. 2. The structure of a 4-ribbon MOS-type GNRFET. A common drain and a common source are shared by the ribbons.

Another bottom-up chemical synthesis approach can produce atomically precise GNRs in different chirality and patterns under 2 nm [26]. Extreme ultraviolet (EUV) lithography is also promising [28]. Further improvement in fabrication technology is necessary to realize mass production of GNR circuits.

Mobility of GNRFETs have been studied [6], [9]. In [9], mobility of a GNRFET with a 2.5 nm-wide GNR is reported to be 171-189 $cm^2/V\cdot s$, calculated based on partial measurements and electrostatic simulations. In [6], GNRFET's mobility is estimated using full-band electron and phonon dispersion relations, and is reported to be $\sim$ 500 $cm^2/V\cdot s$ for 1 nm-wide suspended GNR at room temperature. In our work, channel length is $\sim$ 15 nm and channel width is $\sim$ 1.5 nm. GNRs with this width have a mobility comparable to that of Si-CMOS [6]. Moreover, the mean free path is almost equal to the channel length for such a feature size, and carriers exhibit ballistic transport [6]. Therefore, mobility is less of a concern in this work.

B. Device Structure and Circuit-Level Architecture

Figure 2 shows the structure of the MOS-type GNRFET in our proposed design. In one GNRFET, multiple ribbons are connected in parallel to increase drive strength and to form wide, conducting contacts, as demonstrated in [27], [24] and modeled in [14]. The ribbons are of armchair chirality. Each GNR is intrinsic (undoped) under the gate and is heavily doped with doping fraction f_{dop} between the gate and the wide contact. The doped parts are called *reservoirs*, and the intrinsic part is called the *channel*. The channel is turned on and off by the gate. L_{CH} is channel length, L_{RES} is the reservoir length, W_{CH} is the ribbon width, W_G is the gate width, and $2W_{sp}$ is the spacing between the ribbons.

For every graphene-metal contact, there is a high resistance introduced on the interface, severely degrading circuit performance [29]. As a result, we seek to minimize the number of graphene-metal contacts in our proposed architecture. The proposed circuit design has multiple metal (e.g. Cu) layers on top of a single graphene layer. Channels, drains, and sources of GNRFETs are located on the graphene layer, and gates of GNRFETs are located on the first metal layer. Connections within each logic gate are made on the graphene layer without the need of vias, and the logic gates are connected to each other on the metal layers. At widths above 20 nm, both zigzag and armchair GNRs serve as good conductors, so there is freedom in routing using GNRs as local interconnects on the graphene layer. Vias are assumed to be metal because vertical graphene vias have not been well studied. Note that the

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

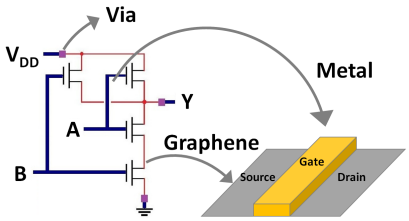


Fig. 3. A *nand2* gate implemented in the proposed architecture of MOS-GNRFET circuits. Inputs A and B, output Y, and power rails V_{DD} and gnd are distributed on the metal layers (bold blue lines). Vias (purple squares) are needed to connect graphene and metal layers. Local interconnects between drains and sources are made of graphene (thin red lines), in order to avoid extra vias.

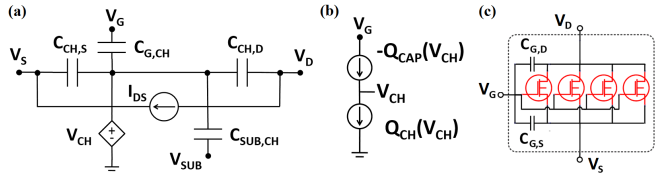


Fig. 4. **(a)** SPICE model of a single GNR. **(b)** SPICE setup for solving Ψ_{CH}. V_{CH} is set to be equal to the channel potential Ψ_{CH}. **(c)** SPICE model of the GNRFET in Figure 2.

use of graphene-metal vias is inevitable because a logic gate output (source/drain) is on the graphene layer, while a logic gate input is on the metal layer; nevertheless, the proposed architecture reduces its usage by connecting sources and drains on the graphene layer. Figure 3 demonstrates the proposed architecture by showcasing a *nand2* gate.

III. Modeling GNRFET and GNR Circuits

This section covers the modeling of GNRFET circuits. In Section III-A, the model of a single GNR ribbon is developed. In Section III-B, a model of a full GNRFET with multiple GNRs is developed, and modeling of vias and graphene interconnects is presented. Note that the discussion focuses on N-type transistors. Similar derivations can be done for P-type transistors.

A. Single GNR Model

Figure 4 (a) shows the equivalent circuit of a single GNR, which is similar to the Si-CMOS SPICE model. Our main challenge is to define equations for all components. I_{DS} models the current flowing through the channel, while the capacitors $C_{CH,D}$, $C_{CH,S}$, $C_{G,CH}$, and $C_{SUB,CH}$ along with the voltage-controlled voltage source V_{CH} are included to model the transient currents that result when the channel charges and discharges. We will derive all the equations in the remainder of this subsection.

1) ***Computing the Subbands****:* A positive subband edge ε_α is given by (1) [7], [13], where N is the number of dimer lines as defined in Section II-A, $t = 2.7$ eV is the tight-binding hopping parameter, α is the subband index ($1 \le \alpha \le N$), and $\delta\varepsilon_\alpha$ is the edge correction factor, given by (2), in which $v = 0.12$ eV is the energy correction of the hopping parameter at the edges in the tight-binding Hamiltonian. A negative subband edge is computed similarly with a negative sign.

$$\varepsilon_\alpha = \left| t \cdot \left(1 + 2\cos\left(\frac{\pi\alpha}{N+1}\right) + \delta\varepsilon_\alpha\right)\right| \tag{1}$$

$$\delta\varepsilon_\alpha = \frac{4vt}{N+1}\cos^2\left(\frac{\pi\alpha}{N+1}\right) \tag{2}$$

The lowest lying subbands dominate the electrostatic and conduction properties [13]. Our experiments show that at most two lowest subbands have a first-order effect on charge and current; hence, our model includes the two lowest subbands for both high accuracy and short computation time. Let α_1 and α_2 be the subband indices corresponding to the two lowest subbands. Let α_0 be a value of α such that $\varepsilon_\alpha = 0$, given by (3). Then, α_1 and α_2 correspond to the two integer values closest to α_0, as in (4). Plugging α_1 and α_2 into (1) gives the subbands.

$$\alpha_0 = \frac{(N+1)\cos^{-1}(-0.5)}{\pi} = \frac{2N+2}{3} \tag{3}$$

$$\alpha_1 = \lfloor \alpha_0 \rfloor; \alpha_2 = \alpha_1 + 1 \tag{4}$$

2) ***Finding Channel Potential*** Ψ_{CH}*:* Let Q_{CH} be the channel charge and Q_{CAP} be the charge across all the capacitors that couple into the channel lumped together. Both Q_{CH} and Q_{CAP} are functions of Ψ_{CH} and have to be equal in magnitude. As a result, equating Q_{CH} and Q_{CAP} yields solution of Ψ_{CH}. In practice, an equation solver (Figure 4 (b)) is constructed in SPICE to solve for Ψ_{CH}. Note that a similar solver was used in the Stanford CNFET Model [16], [17]. Next, we derive Q_{CH} and Q_{CAP}.

3) ***Finding Channel Charge*** Q_{CH}*:* Q_{CH} is derived from carrier density. Electron density n_α in subband α is given by (5). Here, $f(E)$ given by (6) is the Fermi-Dirac distribution function, and $D_\alpha(E)$ given by (7) is the density of states (DOS) in a GNR based on [13]. E is the energy level relative to the conduction band E_C. This implies that $E_C = 0$. E_F is the Fermi level relative to E_C, $\hbar$ is the reduced Plank's constant, and M_α is the effective mass given by (8) [13], k is Boltzmann's constant, T is temperature, and $a = 2.46 \times 10^{-10}$ meters is the lattice constant.

$$n_\alpha = \int_0^\infty f(E) \cdot D_\alpha(E) \mathrm{d}E \tag{5}$$

$$f(E) = \frac{1}{1 + e^{\frac{E-E_F}{kT}}} \tag{6}$$

$$D_\alpha(E) = \frac{2\sqrt{M_\alpha}}{\pi\hbar} \cdot \frac{\varepsilon_\alpha + E}{\sqrt{\varepsilon_\alpha E(E + 2\varepsilon_\alpha)}} \tag{7}$$

$$M_\alpha = \frac{2\hbar^2\varepsilon_\alpha}{3a^2t^2 \cdot \cos(\frac{\pi\alpha}{N+1})} \tag{8}$$

The integral in (5) has no closed-form solution. A closed-form approximation was derived in [13] by approximating $f(E)$ with Boltzmann distribution $\exp((E_F - E)/kT)$, which is valid when $E - E_F > 3kT$. Since GNRs may have a low subband, the approximation is not always accurate. Therefore,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

we need to derive an expression valid for all possible E. Since (5) cannot be solved directly, we approximate $f(E)$ with an exponential function when $E_F - E_C < 0$, a step function when $E_F - E_C > 2kT$, and a smoothing function when $E_F - E_C$ is in between.

*a) **Exponential Approximation**:* Here, $f(E)$ is approximated by a decaying exponential function $f'(E)$ [30] as follows:

$$f(E) \sim f'(E) = f(0) \cdot e^{\frac{-E}{\beta kT}} \tag{9}$$

where β is chosen such that $f(3kT) = f'(3kT)$ and is given by

$$\beta(E_{FC}) = \frac{3}{\ln f(-E_{FC}) \cdot \left[1 + \exp(\frac{3kT - E_{FC}}{kT})\right]} \tag{10}$$

where $E_{FC} = E_F - E_C$. Since $E_C = 0$, $E_{FC} = E_F$. Note that we have $f(E) = f'(E)$ on the conduction band ($E = E_C = 0$) such that $f'(E)$ approximates $f(E)$ very well when $E \sim E_C$. Since DOS $D_\alpha(E)$ is highest near the conduction band, this gives an accurate estimation of n_α. Electron density computed with this approximation is denoted $n_{\alpha,exp}$ and is given by

$$n_{\alpha,exp}(E_{FC}) = \frac{\sqrt{M_\alpha(\beta kT)^3}\left(1 + \frac{2\varepsilon_\alpha}{\beta kT}\right)}{2\pi\hbar\varepsilon_\alpha} \cdot e^{\frac{E_{FC}}{\beta kT}} \tag{11}$$

*b) **Step Approximation**:* When $E_F > 3kT$, $f(E) \sim 1$ as $E \sim E_C$. Since DOS $D_\alpha(E)$ is highest in this region, approximating the Fermi-Dirac distribution as a step function (1 when $E \leq E_F$ and 0 when $E > E_F$) provides a good approximation of electron density. Electron density computed with this approximation is denoted $n_{\alpha,step}$ and is given by

$$\begin{aligned} n_{\alpha,step}(E_{FC}) &= \int_0^{E_F} 1 \cdot D_\alpha(E)\mathrm{d}E \\ &= \frac{2\sqrt{M_\alpha}}{\pi\hbar}\sqrt{\max\left(\frac{E_{FC}(E_{FC} + 2\varepsilon_\alpha)}{\varepsilon_\alpha}, 0\right)} \end{aligned} \tag{12}$$

Note that for $E_F - E_C < 0$, the expression evaluates to 0.

*c) **Combined Approximation**:* We have derived two expressions that approximate electron density n_α under different conditions. To obtain a smooth, continuous charge function, n_α is expressed as a weighted sum of the two approximations as in (13), where m is the relative weight defined in (14). To make the expressions more general, E_{FC} is introduced. Note that if $E_{FC} = kT$, both approximations are weighted equally. The exponential approximation dominates when $E_{FC} < 0$, while the step approximation dominates when $E_{FC} > 2kT$.

$$n_\alpha(E_{FC}) = m \cdot n_{\alpha,exp}(E_{FC}) + (1 - m)n_{\alpha,step}(E_{FC}) \tag{13}$$

$$m = \frac{1}{1 + e^{\frac{3(E_{FC} - kT)}{kT}}} \tag{14}$$

The effectiveness of (13) was tested and validated in the range $0.1 < \varepsilon_\alpha < 0.5$. The case where $\varepsilon_\alpha = 0.3$ eV (corresponding to $N = 12$) is shown in Figure 5, where *Numerical* was obtained by evaluating the integral in (5), *Boltzmann* was obtained from expressions in [13], *Exponential* was obtained from (11), and *Combined* was obtained from (13). All three expressions match *Numerical* when E_{FC} is small. However, as E_{FC} increases, both *Exponential* and *Boltzmann* fail, while *Combined* is accurate throughout the entire range. This is because the combined approximation gives an accurate Fermi level over the entire range, while the exponential and Boltzmann approximations do not.

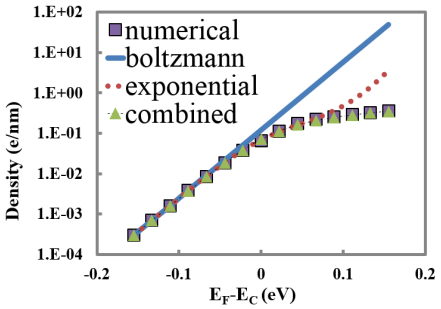


Fig. 5. Charge density n_α vs $E_F - E_C$ in the case of $\varepsilon_\alpha = 0.3eV$ ($N = 12$).

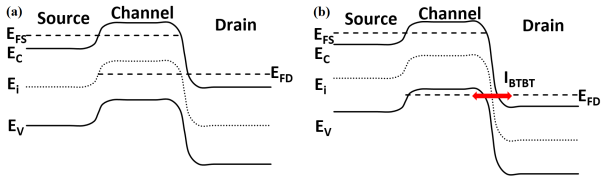


Fig. 6. Typical band diagrams of a GNRFET **(a)** under low V_{DS} and **(b)** under high V_{DS}. In (b), the band bending is high enough to induce band-to-band tunneling current (I_{BTBT}).

*d) **Computing Channel Charge** Q_{CH}:* Total channel charge Q_{CH} is derived by analyzing the band diagram. Figure 6 (a) shows a band diagram where GNRFET is biased at $V_{GS} > 0$ and $V_{DS} > 0$. Fermi levels at the source and the drain are denoted E_{FS} and E_{FD}, respectively. Since $V_{DS} > 0$, $E_{FD} < E_{FS}$. Because the source and the drain are heavily doped and have high electron densities, E_{FS} and E_{FD} are both above the conduction band.

Holes are negligible in the channel when V_{DS} is low. However, as V_{DS} increases, the conduction band on the drain side ($E_{C,D}$) goes below the valence band in the channel ($E_{V,CH}$), and holes tunnel from the drain into the channel. The tunneling probability $Tr(\Psi_{CH,D})$ is given by (15), where $\Psi_{CH,D}$ is the amount of band bending between channel and drain, $\eta_{0.5}$ is a fitting parameter adjusting the amount of band bending such that $Tr = 0.5$ when $\Psi_{CH,D} > E_G = E_C - E_V$, γ is another fitting parameter controlling how fast Tr increases as $\Psi_{CH,D}$ increases. The equation takes the form of a sigmoid function that smoothly transitions from 0 to 1 at the onset where band-to-band tunneling starts taking place. Note that $\eta_{0.5}$ and γ only need to be obtained once and are valid throughout different devices at different biases. In our implementation, $\eta_{0.5} = 0.6$ and $\gamma = 1/6$. The equation and the parameters are obtained by experimenting with channel charge data extracted from NanoTCAD ViDES [11] that could not be accounted for by the majority carrier contribution alone.

$$Tr(\Psi_{CH,D}) = \left(1 + e^{\frac{(2+\eta_{0.5})\varepsilon_\alpha - q\Psi_{CH,D}}{\gamma\varepsilon_\alpha}}\right)^{-1} \tag{15}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

The final expression of Q_{CH} (16) is obtained by summing up electron and hole densities and multiplying by electron charge q. The channel potential Ψ_{CH} is the negative of the intrinsic energy level E_i. Therefore, the conduction band is $E_C = \varepsilon_\alpha - q\Psi_{CH}$, and the valence band $E_V = -\varepsilon_\alpha - q\Psi_{CH}$. Also, the Fermi level at source/drain equals to the applied voltage. Thus, $E_{FS} - E_C = -qV_S - (\varepsilon_\alpha - q\Psi_{CH})$.

$$\begin{aligned} Q_{CH}(\Psi_{CH}, V_D, V_S) = \frac{qL_{CH}}{2} \sum_\alpha [&-n_\alpha(q\Psi_{CH} - \varepsilon_\alpha - qV_S) \\ &-n_\alpha(q\Psi_{CH} - \varepsilon_\alpha - qV_D) \\ &+Tr(\Psi_{CH,D}) \cdot p_\alpha(qV_D - q\Psi_{CH} - \varepsilon_\alpha)] \end{aligned} \quad (16)$$

*4) **Finding** Q_{CAP}:* Q_{CAP} (17) is composed of several parts. $C_{G,CH}$ and $C_{SUB,CH}$ are physical capacitors that model the coupling between gate/channel and channel/substrate, respectively, empirically modeled by (18). $C_{DIBL,D}$ and $C_{DIBL,S}$ are effective capacitors that model the drain-induced barrier-lowering (DIBL) effect. They were empirically modeled as $0.15C_{G,CH} \cdot Tr$ and $0.05C_{G,CH}$, respectively. V_{FB} is the flat-band voltage, the work function difference between metal and graphene. ϵ_r is the relative permittivity of the gate oxide material.

$$\begin{aligned} Q_{CAP} &= C_{G,CH}(V_G - V_{FB} - \Psi_{CH}) \\ &+ C_{SUB,CH}(V_{SUB} - V_{FB} - \Psi_{CH}) \\ &+ C_{DIBL,D}(V_D - \Psi_{CH}) + C_{DIBL,S}(V_S - \Psi_{CH}) \end{aligned} \quad (17)$$

$$C_{G(SUB),CH} = \frac{5.55 \times 10^{-11} \epsilon_r L_{CH}}{\left(1 + \frac{1.5T_{ox}}{W_G}\right) \ln\left(\frac{5.98W_{CH}}{0.8T_{ox}}\right)} \quad (18)$$

*5) **Intrinsic Capacitors**:* By definition, $C_{CH,D} = \partial Q_{CH}/\partial V_D$ and $C_{CH,S} = \partial Q_{CH}/\partial V_S$. They were implemented in SPICE as voltage-controlled capacitors by defining the charge equation.

*6) **Current Modeling**:* Given Ψ_{CH}, the electron current I_e is computed from (19) based on the Landauer-Buttiker formalism [13], [15]. Here, h is Plank's constant, and $f(\cdot)$ is the Fermi-Dirac distribution. $T(E)$ is the tunneling probability. In the case of thermionic conduction, $T(E) = 1$. $E_{FD,C}$ ($E_{FS,C}$) is the difference between the E_C in the channel and E_F on the drain (source) side, as in Figure 6. Essentially, the probability of electrons being injected into the conduction band from the source is subtracted from the probability of electrons being injected into the conduction band from the drain. By recognizing the Fermi-Dirac integral of order 0 [30], (19) can be evaluated analytically, which yields (20). In an N-type GNRFET, $I_{DS} = I_e$, while in a P-type GNRFET, $I_{DS} = I_h$, which is obtained similarly.

$$I_e = \frac{2q}{h} \sum_\alpha \int_0^\infty T(E) \left[f(E - E_{FS,C}) - f(E - E_{FD,C})\right] \mathrm{d}E \quad (19)$$

$$\begin{aligned} I_e(\Psi_{CH}, V_D, V_S) = \frac{2qkT}{h} \sum_\alpha \Bigg[&\ln\left(1 + e^{\frac{q(\Psi_{CH} - V_S) - \varepsilon_\alpha}{kT}}\right) \\ &- \ln\left(1 + e^{\frac{q(\Psi_{CH} - V_D) - \varepsilon_\alpha}{kT}}\right)\Bigg] \end{aligned} \quad (20)$$

*7) **Considering Band-to-Band Tunneling**:* When V_{DS} is high enough to incur significant band bending, the band-to-band tunneling (BTBT) effect starts to occur in the channel, contributing to additional current. Figure 6 (b) shows a band diagram with significant band bending such that BTBT occurs. It sometimes contributes to leakage current [31]. We took a similar approach to the work of [16] and [32] of CNFETs to model the BTBT current in GNRFETs, which is also based on the Landauer-Buttiker equation (19), with $T(E)$ representing the BTBT probability. The resulting BTBT current becomes (21). T_{BTBT} is the tunneling probability, expressed as (22). $\Psi_{bi} = 0.4$ is the built-in potential. l_{relax} is the distance for the potential drop across the drain-channel junction to relax.

$$I_{BTBT} = \frac{4qkT}{h} \sum_\alpha T_{BTBT} \left[\ln \frac{1 + e^{\frac{q(V_D - V_S) - \varepsilon_\alpha - q\Psi_{bi}}{kT}}}{1 + e^{\frac{-\varepsilon_\alpha - q\Psi_{bi}}{kT}}}\right] \quad (21)$$

$$T_{BTBT} = \frac{-\pi^3 \cdot \sqrt{M_\alpha}(0.5\varepsilon_\alpha)^{1.5}}{9\hbar\sqrt{q}\left(\frac{q(V_D - \Psi_{CH} + V_S + \Psi_{bi})}{l_{relax}}\right)} \quad (22)$$

*8) **Considering Line Edge Roughness**:* To date, fabrication technology cannot produce GNRs with perfectly smooth edges. The uneven edges result in a phenomenon called *line edge roughness*, which affects the properties of GNRs. Line edge roughness is characterized by p_r, the probability that any atom on the edges of a GNR is removed, as in [11]. The removal of atoms has two effects: 1) Subbands (1) varies throughout the channel as N is no longer constant. 2) Ballistic transport is disrupted. These effects strongly depend on which atoms are removed [11]; hence, numerical simulations are required for the most accurate analysis. Nevertheless, we are able to model the trend as p_r varies and evaluate the effect of line edge roughness on the circuit level.

To model the varying width, we introduce the concept of an effective subband edge $\varepsilon_{\alpha,eff}$ given by (23), where $\varepsilon_{\alpha,N}$ is the ε_α for a given N. In a unit segment of GNR, there are 8 atoms (shown as red dots in Figure 1) that would reduce N by 1 if removed. Therefore, the probability of N remaining unchanged is $(1 - p_r)^8$. And $\varepsilon_{\alpha,eff}$ is the weighted average of $\varepsilon_{\alpha,N}$ and $\varepsilon_{\alpha,N-1}$, given by (23). The scattering coefficient A is introduced to account for the current reduction due to disrupted ballistic transport. It is empirically modeled as (24).

$$\varepsilon_{\alpha,eff} = (1 - p_r)^8 \varepsilon_{\alpha,N} + 1(1 - (1 - p_r)^8)\varepsilon_{\alpha,N-1} \quad (23)$$

$$A = 0.98(1 - 4p_r)^6 + 0.02 \quad (24)$$

The current equations derived in Sections III-A6 and III-A7 assumes ballistic transport and are denoted as $I_{bal} = I_e + I_{BTBT}$ combined. Current with line edge roughness present, I_{rough}, is derived from I_{bal} and is modeled as follows:

$$I_{rough} = A \cdot I_{bal}(\varepsilon_{\alpha,eff}) \quad (25)$$

B. Full GNRFET Model, Vias, and Interconnects

Figure 4 (c) shows the SPICE implementation of a GNRFET with four parallel GNRs equivalent to that in Figure 2. Each transistor highlighted in red corresponds to an individual GNR, which is modeled by the circuit in Figure 4. C_{GD} and C_{GS}, given by (26), are parasitics introduced by the fringing fields between the gate and the reservoirs. They are modeled empirically based on data from FastCap [33]. When two GNRFETs are connected, graphene-metal contact resistance exists externally between gates and drains/sources.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

$$C_{GD} = C_{GS} = 1.26 \times 10^{-10} W_G (0.8 - 0.2T_{ox} + 0.015T_{ox}^2) \quad (26)$$

The local GNR interconnects (20 nm wide) between transistors are much shorter than the mean free path of graphene and have negligible resistance. For this reason, resistance of interconnects within logic gates is neglected in a first-order model, as in [14]. On the other hand, the impact of the graphene/metal contact resistance introduced by vias is significant. The contact resistance is modeled based on experimental results from [29].

C. Discussion on Model Empiricism

In summary, empirical parameters occur in our model in the following situations:

1) Smoothing functions for the transitions in (13), (15).
2) Capacitance equations (18) and (26). As GNRFETs do not have a simple parallel plate capacitor structure, we resorted to empirical modeling based on data collected from FastCap.
3) Capacitance for modeling DIBL.
4) Line edge roughness scattering coefficient.

It is possible to replace the empirical equations and parameters if more accurate description is found. In particular, should the device geometry differ from our default design by a great deal, the users may use FastCap to obtain new capacitance values that suit their design better.

D. Note on Gummel Symmetry Test

Gummel Symmetry Test (GST) is a common test on compact models. The transistor is biased with a fixed V_{GS} and V_{BS}, and V_D and V_S are set to V_x and $-V_x$, respectively. Then, the drain-source current I is measured under a sweep of V_x. For a model to pass GST, it needs to satisfy two criteria: 1) the symmetry on the drain and the source of the transistor, i.e. $I(V_x)$ is an odd function and 2) no singularity occurs at V_x = 0 (by checking the continuity of higher order derivatives). GST is particularly important for a compact model to be used in the distortion analysis in analog circuits, but it is not a strict requirement for other applications [34].

Figure 7 shows the current and derivatives vs. V_x relationship near $V_x = 0$. It shows that despite the continuity, the current is not symmetric, i.e., the drain and source in our model are not interchangeable. This is due to the fact that some of the equations we developed are not identical for drain and source. In particular, our modeling of DIBL and BTBT is based on the assumption that $V_D > V_S$ and that these effects are much more significant on the drain side. A compact model of CNFET similar to ours also does not feature interchangeable drain and source [16], [17]. Despite this limitation, the model is perfectly fine for digital circuits designed under the prevalent complementary-symmetry metal-oxide-semiconductor (CMOS) style.

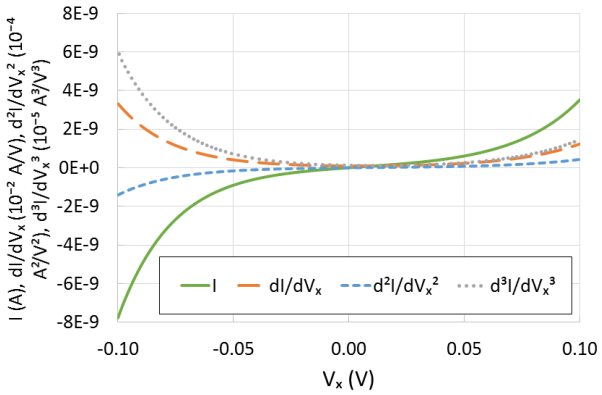


Fig. 7. Gummel Symmetry Test of our GNRFET model, showing I, $\frac{dI}{dV_x}$, $\frac{d^2I}{dV_x^2}$, and $\frac{d^3I}{dV_x^3}$ vs. V_x from V_x = -0.1 to 0.1 V.

IV. Experimental Results

The equivalent circuit model and all equations in Section III were implemented in HSPICE as a *subckt*. The work [35] analyzes how a generic CNT/graphene transistor *subckt* is processed in SPICE. In Section IV-A, the compact model is validated against numerical simulation in NanoTCAD ViDES [11], [22] and compared with measurement data from fabricated GNRFETs. With the accuracy of our SPICE model thoroughly validated, we can proceed with SPICE simulations of GNRFET and GNR-based circuits. This gives insightful information on how GNR-based circuits would perform once fabrication techniques become mature. In Sections IV-B, IV-C and IV-D, we implemented digital logic gates with our GNRFET SPICE model, performed transistor- and circuit-level analyses, and compared them with those implemented in Si-CMOS 16-nm high-performance (HP) and low-power (LP) libraries from Predictive Technology Models (PTM) [36]. In particular, Section IV-D focuses on the effect of process variation based on Monte Carlo simulations.

A. Transistor Model Validation

1) ***Default Device****:* First, we simulated a GNRFET with parameters $N = 12$, $L_{CH} = 15$ nm, $L_{RES} = 10$ nm, $T_{ox} = 1$ nm, $f_{dop} = 0.005$, and $V_{FB} = 0$, which is the default device setting in ViDES. The I-V curves of the GNRFET biased at $0 \leq V_{GS} \leq 0.8V$ and $0 \leq V_{DS} \leq 0.8$ V are plotted in Figure 8, in which *num* stands for ViDES and *ana* stands for our model. The voltage range is chosen by assuming a maximum supply voltage $V_{DD} = 0.8$ V, similar to that in the Si-CMOS 16-nm technology ($0.7 - 0.9$ V). It is shown that our model agrees very well with numerical simulations. By defining $I_{on} = I(V_{GS} = V_{DS} = V_{DD})$ and $I_{off} = I(V_{GS} = 0, V_{DS} = V_{DD})$, it can be observed that the I_{on}/I_{off} ratio is reduced at higher V_{DS}. This is caused by an increased Ψ_{CH} due to high V_{DS}. This also serves as a guideline of choosing V_{DD} as it cannot be raised too high in order to maintain a high I_{on}/I_{off} ratio suitable for digital applications. While a low V_{DD} gives a higher subthreshold swing, the I_{on}/I_{off} ratio reaches maximum around $V_{DD} = 0.5$V.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

*2) **Variation in Design Parameters**:* Next, we validated that the model responds correctly to changes in design parameters, specifically, N, f_{dop}, T_{ox}, and p_r. I_{on} and I_{off} at $V_{DD} = 0.5$ V were computed at various settings in our model and in ViDES.

Figure 9 shows the effect of N. Our model tracks the periodic effect on band gaps discussed in [7]. For $N = 8, 11, 14$, and 17, the band gap is very small, resulting in a low I_{on}/I_{off} ratio. For $N = 6, 9, 12, 15$, and 18, there is a moderate band gap, which results in a high I_{on}/I_{off} ratio and a high I_{on}. For $N = 7, 10, 13$, and 16, the band gap is the largest, which results in the highest I_{on}/I_{off} ratio. However, I_{on} is still low because the channel is never fully enhanced. Also note that the I_{on}/I_{off} ratio tends to increase as N decreases.

Figure 10 shows the effect of f_{dop}. Doping affects the band bending between the channel and the drain $\Psi_{CH,D}$, and further controls Tr and I_{DS}. Figure 11 shows the effect of T_{ox}. T_{ox} is inversely correlated to $C_{G,CH}$; a smaller T_{ox} implies a larger $C_{G,CH}$, which provides a better control of Ψ_{CH}. Thus, I_{on} is increased and I_{off} is reduced as T_{ox} decreases. Figure 12 shows the effect of line edge roughness in terms of p_r. Edge roughness reduces I_{on}. It also reduces band gaps, which leads to an increase in I_{off}. Even though our model does not match the ViDES data perfectly, it captures the deterioration of the I_{on}/I_{off} ratio as line edge roughness is increased.

*3) **Comparison with Measurement Data from Fabricated GNRFETs**:* Among all existing work on fabricated GNRFETs, the single-layer SB-type GNRFET in [9] with W $\sim$ 2 nm is closest to our target range of design parameters. Most of other works evaluated their GNRFETs under high V_{GS} range (e.g., up to 40V) [23], [24], [25], [27]. In [12], a comparison between SB-type and MOSFET-type GNRFETs showed that SB-type FETs have up to 50% lower current than MOSFET-type ones.

We conducted a similar comparison between the fabricated device in [9] and a $N = 16$ MOS-type GNRFET with $p_r = 0.1$ in order to account for the line edge roughness (effective $W = 2.1$ nm). For I_{on} and I_{off} with $V_{DS} = 10$ mV, 0.1 V, and 0.5 V respectively across a 2-V range of V_{GS}, the error is within a range of 25% to 100%. The sources of error include the following: 1) The effect of Schottky barriers. 2) Fabricated GNRs do not have a well-defined N, making it difficult for a direct comparison. 3) Current fabricated GNRs have unpredictable width variation and line edge roughness. 4) Our model assumes ballistic transport, while the fabricated GNRs in [9] have lengths $>$ 100 nm, greater than the mean free path. 5) Other experimental settings and nonidealities that are unclear to us.

Note that in [9], an *edge scattering probability* 20% was calculated, which is the probability of back-scattering that depends on the edge quality, while we used the probability of an atom on the edge being missing as the *line edge roughness probability*. This terminology was defined in the open-source NanoTCAD ViDES [11][22], which we used to produce validation data points, and therefore we adopted this probability in our model. We did not find a straight-forward relation between the two probabilities, but we were able to compare our model with the data reported in [9] by using a line edge roughness of 10%. Furthermore, as indicated in Figure 11 of our paper, a line edge roughness of 20% leads to a poor I_{on}/I_{off} ratio of less than 10, which is not the case in the work of [9] where the I_{on}/I_{off} is greater than 10^6. Therefore, we believe simulating a 10% line edge roughness is sufficient in the experiments in all the following subsections.

B. Transistor-Level Properties

In this section, we review the transistor-level characteristics of MOS-GNRFETs. Based on the explorations in [14] and Section IV-A, MOS-GNRFETs work well under a low V_{DD} around 0.5 V. Therefore, we choose a nominal $V_{DD} = 0.5$ V in all the following experiments unless otherwise stated. Also based on the explorations in Section IV-A, we choose the design parameters as follows: $N = 12$, $f_{dop} = 0.001$, $T_{ox} = 0.95$ nm, and $L_{CH} = 16$ nm.

Figure 13 shows the I-V curves of MOS-GNRFET as well as the 16-nm Si-CMOS (HP) and 16-nm Si-CMOS (LP) transistors from PTM for comparison. The transistor dimensions of the GNRFETs are scaled to match the PTM libraries. Overall, Si-CMOS (HP) has the highest current, and the Si-CMOS (LP) has the lowest. MOS-GNRFET and Si-CMOS (LP) have better I_{on}/I_{off} ratios than Si-CMOS (HP).

Table I shows the subthreshold swing S and I_{on}/I_{off} ratio of each device under respectively chosen V_{DD}. It is shown that ideal MOS-GNRFETs have the lowest subthreshold swing (66.67 mV/dec)and the highest I_{on}/I_{off} ratio (1.81 ^{5}). However, as line edge roughness comes into play, the subthreshold swing increases to 140.85 mV/dec, and the I_{on}/I_{off} ratio drops to 98.5. In other words, the transistor characteristics become comparable or even worse than Si-CMOS.

TABLE I
TRANSISTOR PROPERTIES

Device	p_r	S (mV/dec)	I_{on}/I_{off}	V_{DD} (V)
Si-CMOS (HP)	–	93.46	3.49E+03	0.7
Si-CMOS (LP)	–	86.96	5.12E+06	0.9
MOS-GNRFET	0	66.67	1.81E+05	0.5
	0.05	83.33	3.69E+03	0.5
	0.1	140.85	9.85E+01	0.5

Subthreshold swing and I_{on}/I_{off} ratio of each device. For GNRFETs, devices of different line edge roughness (p_r) are listed as well.

C. Circuit-Level Evaluation

We performed HSPICE DC and transient analyses on digital circuits defined in SPICE netlists. We used an input slew of 10 ps and an output load of 1 fF. We first evaluated the noise margin of an inverter. Then, we evaluated delay and power of a buffer chain under various supply voltages to understand the power-delay trade-off. Next, the buffer chain is simulated with various design parameters such as N, f_{dop}, T_{ox}, and L_{CH} to evaluate the impact of process variation. Following is a thorough comparison performed on a set of digital benchmark circuits implemented with MOS-GNRFET and Si-CMOS under their respective optimal settings. Finally, we performed Monte Carlo simulations to investigate the impact of process variation on GNRFET circuits.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

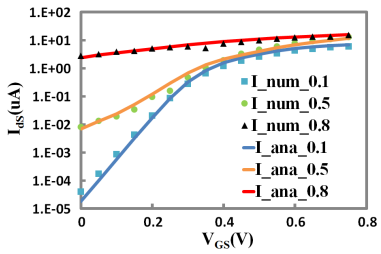


Fig. 8. I_{DS} vs V_{GS} with V_{DS} 0.1, 0.5, 0.8 V in an N-type GNRFET.

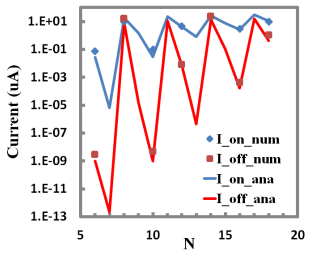


Fig. 9. (I_{on} and I_{off}) vs N. Note that ViDES only supports even N.

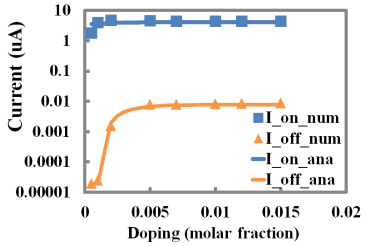


Fig. 10. (I_{on} and I_{off}) vs f_{dop}, doping fraction in reservoirs.

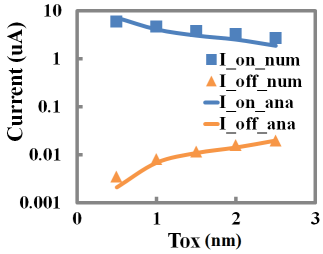


Fig. 11. (I_{on} and I_{off}) vs T_{ox}, oxide thickness.

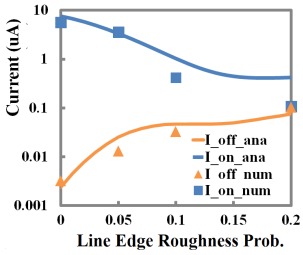


Fig. 12. (I_{on} and I_{off}) vs p_r, line edge roughness probability.

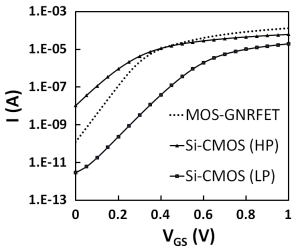


Fig. 13. I_{DS} vs V_{GS} for MOS-GNRFET, 16-nm High-Performance Si-CMOS, 16-nm Low-Power Si-CMOS, respectively.

1) Noise Margin Analysis: Figure 14 shows the voltage transfer curves of inverters built with MOS-GNRFETs with different settings, namely, ideal MOS-GNRFETs (with no graphene-metal contact resistance), MOS-GNRFETs with graphene-metal contact resistance, and MOS-GNRFETs with graphene-metal contacts and line edge roughness ($p_r = 5\%$ and $p_r = 10\%$, respectively). V_{in} and V_{out} are the input and output voltages of the inverter, respectively. All inverters have full voltage swings. The ranges of V_{in} that result in correct operations are indicated by V_{IL} and V_{IH}, the maximum voltage for a valid low input and the minimum voltage for a valid high input, respectively. V_{IL} and V_{IH} are specifically measured as the points with slopes equal to 1. Table II shows the V_{IL}, V_{IH}, and the normalized voltage range of correct inverter operation. The ideal MOS-GNRFET inverter has a sharp voltage transfer curve, which makes it more robust, as V_{out} almost stays the same as V_{in} approaches V_{IL} or V_{IH}. Contact resistance on MOS-GNRFETs with $p_r = 0\%$ does not have much impact on the voltage transfer curve. On the other hand, line edge roughness significantly reduces the region of correct operation.

TABLE II
NOISE MARGIN OF INVERTERS

Device	p_r	V_{IL} (V)	V_{IH} (V)	NM/V_{DD}
MOS-GNRFET	0	0.2336	0.2664	0.9344
MOS-GNRFET w/ Res	0	0.2328	0.2672	0.9312
	0.05	0.2255	0.2746	0.9018
	0.1	0.2151	0.2849	0.8604

V_{IL}, V_{IH}, and the normalized voltage range of correct operations of inverters (indicated by noise margin divided by V_{DD}) measured on MOS-GNRFET inverters with different settings.

2) Impact of Supply Voltage: We evaluated the delay and power of a 7-stage, fanout-of-4 buffer chain under various supply voltages to understand the power-delay trade-off. The

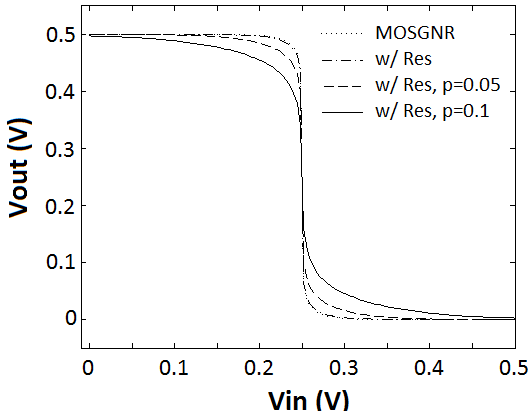


Fig. 14. Voltage transfer curves of MOS-GNRFETs with different settings. Both inverters have full voltage swings. For the MOS-GNRFET inverter, V_{IL} = 0.23 V, V_{OL} = 0.27 V, and the noise margin is 92% of V_{DD}. Note that the curves of MOS-GNRFET with no line edge roughness, whether with contact resistance or not, almost overlap with each other.

buffer chain was implemented in Si-CMOS (LP), Si-CMOS (HP), ideal MOS-GNRFETs (with no graphene-metal contact resistance), MOS-GNRFETs with graphene-metal contact resistance, and MOS-GNRFETs with graphene-metal contacts and line edge roughness. We implemented Si-CMOS with the 16-nm HP and LP libraries from PTM, and implemented MOS-GNRFETs with our SPICE model. The minimum-size MOS-GNRFET is set to have 6 ribbons in order to match the dimensions of Si-CMOS. Graphene-metal junctions are present in circuit layouts, as discussed in Section II-B, and they are modeled with a 20-kΩ resistor by assuming a 50-nm via width [29]. Limitations on fabrication techniques contribute to line edge roughness. We simulated the cases of $p_r = 5\%$ and 10%. Considering graphene-metal contacts and line edge roughness makes our simulations closer to reality. The ideal MOS-GNRFET, although not realistic, gives an upper bound

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

on circuit performance.

Figure 15 shows the impact of supply voltage V_{DD} on the circuit performance. The metrics reported are delay, dynamic power, leakage power, total power, and energy-delay product (EDP). Delay is measured as the maximum propagation delay from a series of random input vectors. Dynamic power is measured based on the assumption that the circuits operates at a frequency based on the maximum propagation delay. Graphene-metal contact resistance and line edge roughness are nearly inevitable in practice, and they significantly increase delay and leakage power. The optimal operating V_{DD} is around 0.5 V, if delay, dynamic power, and leakage power are all considered.

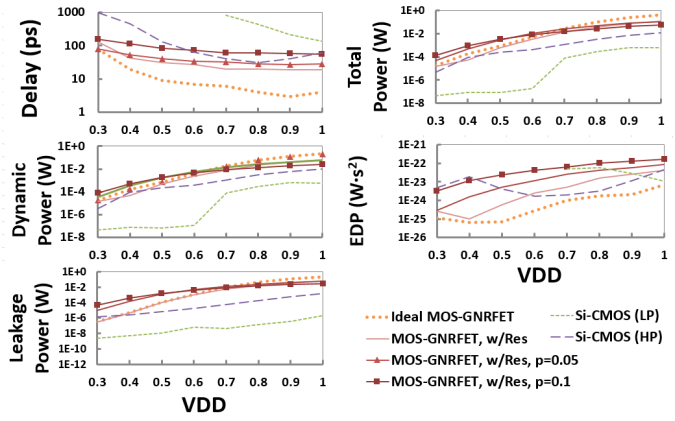


Fig. 15. Delay, dynamic power, leakage power, total power, and EDP vs V_{DD}.

3) Impact of Design Parameters: Process variation on GNRFETs will result in fluctuations in W_{CH}, L_{CH}, T_{ox}, and f_{dop}. To evaluate the impacts on circuit performance due to these variations, we performed a series of SPICE simulations on the buffer chain in Section IV-C2 by varying these design parameters to find their respective impacts on the circuit level.

Figure 16 shows the impact of ribbon width N (W_{CH}). The results are consistent with the periodic band gaps in terms of N as reported in [7]. For examples, $N = 3p + 2$ (8, 11, 14) gives a small band gap, resulting in almost equally high I_{on} and I_{off}, corresponding to low delay and high power. $N = 3p + 1$ (10, 13, 16) gives the largest band gap with low I_{on} and very low I_{off}, resulting in the highest I_{on}/I_{off} ratio. Therefore, the power, especially the leakage power, is the lowest. $N = 3p$ (9, 12, 15) gives a moderate band gap, and the delay and power performance is between the other two cases, with EDP being the lowest. Under the influence of line edge roughness, the effective band gaps fall between the band gaps corresponding to an effective width N_{eff} between N and $N-2$, making the periodic effect not so significant. Also, the scattering effect causes the current to drop. As a result, delay is generally higher and power is generally lower compared to the ideal cases. It is noteworthy that the I_{on}/I_{off} ratio in the case of $N = 3p + 2$ is extremely small and results in poor transistor operation. For example, Figure 17 shows an inverter with MOS-GNRFET of $N = 14$, with output voltage ranging from 0.074 V to 0.426 V, not reaching full swing. V_{IL} and V_{IH} in this case are 0.2801 V and 0.2199 V, respectively, making the noise margin 88% of V_{DD}. This observation is consistent with the transistor-level NEGF simulation results reported in [11]. In short, variation in ribbon width can cause significant performance degradation and is a possible major drawback for GNRFETs.

The effects of other parameters, L_{CH}, T_{ox}, and f_{dop}, are shown in Figure 18. Among L_{CH}, T_{ox}, and f_{dop}, L_{CH} has the least effect, T_{ox} has an impact on everything, and f_{dop} greatly changes the leakage power. Gate input capacitance is related to L_{CH} and T_{ox}. I_{on} is affected by T_{ox}. Doping mainly controls I_{off}. I_{on} and input capacitance affect delays. I_{off} contributes to leakage power. In general, changes in T_{ox} or L_{CH} affect delay, power, or EDP only within one order of magnitude. On the other hand, line edge roughness has a very high impact on delay and power. These observations are consistent with our model.

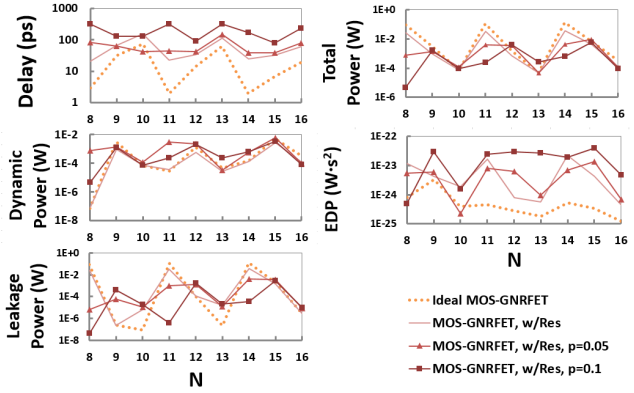


Fig. 16. Delay, dynamic power, leakage power, total power, and EDP vs N.

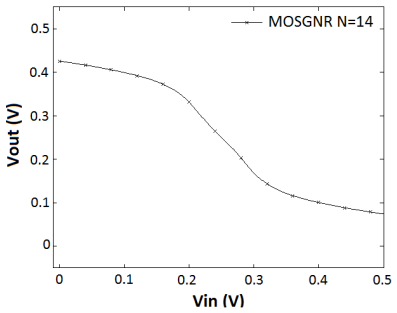


Fig. 17. Voltage transfer curve of an inverter with MOS-GNRFET of $N = 14$, showing poor performance.

4) Performance Comparison Between GNRFET and Si-CMOS: We compared delay and power performance on a set of digital circuits, implemented with Si-CMOS and MOS-GNRFETs, respectively.

We first evaluated the delay and power of basic logic gates such as *inv*, *nand2*, *nor2*, *nand3*, *nor3*, *nand4*, *xor2*, and a 7-stage, fanout-of-4 buffer chain, which were implemented in Si-CMOS, ideal MOS-GNRFETs (with no graphene-metal contact resistance), MOS-GNRFETs with graphene-metal contact resistance, and MOS-GNRFETs with graphene-metal contacts and line edge roughness. We implemented Si-CMOS with the 16-nm LP and HP libraries from PTM, and implemented MOS-GNRFETs with our SPICE model. The minimum-size

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

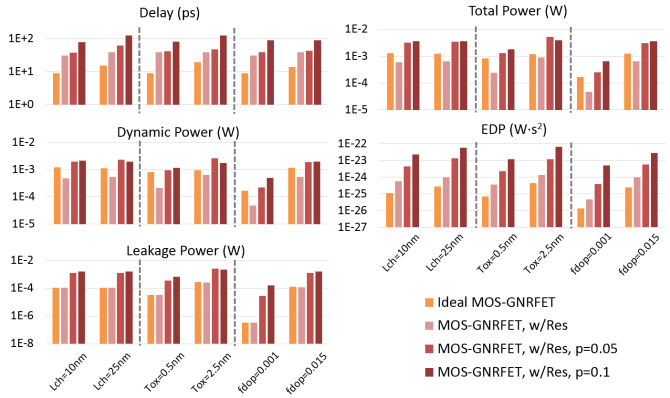


Fig. 18. Delay, dynamic power, leakage power, total power, and EDP vs L_{CH}, T_{ox}, and f_{dop}.

MOS-GNRFET was set to have 6 ribbons in order to match the dimensions of Si-CMOS. Gate sizing was done to balance the pull-up and pull-down networks in the logic gates. Graphene-metal junctions are present in circuit layouts, as discussed in Section II-B, and they are modeled with a 20-kΩ resistor by assuming a 50-nm via width. We simulated the cases of $p_r = 5\%$ and 10%. For Si-CMOS, V_{DD} was chosen as the nominal V_{DD} recommended by PTM, which is 0.9 V for LP and 0.7 V for HP. The V_{DD} of MOS-GNRFET was chosen to be 0.5 V, according to the exploration in Section IV-C2. The doping fraction of MOS-GNRFET was chosen to be 0.001, according to the exploration in Section IV-C3. Figure 19 shows the delay and power evaluation results of the basic logic gates.

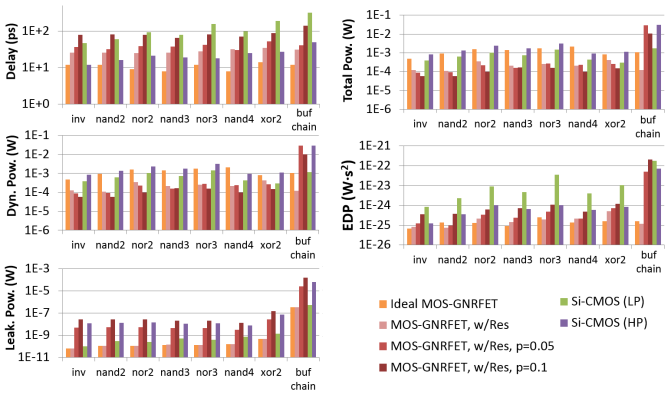


Fig. 19. Simulation of basic logic gates, reporting delay, dynamic power, leakage power, total power, and EDP.

Next, we simulated a set of benchmark circuits under four settings: MOS-GNRFET with graphene-metal contacts and $p_r = 0\%$, MOS-GNRFET with graphene-metal contacts and $p_r = 10\%$, Si-CMOS (LP), and Si-CMOS(HP). Considering the fact that graphene-metal contact resistance cannot be avoided in the circuit architecture discussed in II-B, we did not simulate ideal MOS-GNRFET without contact resistance here. Also, the performance of MOS-GNRFET with $p_r = 5\%$ normally lies between that of MOS-GNRFET with $p_r = 0\%$ and MOS-GNRFET with $p_r = 10\%$, so we did not simulate this case. The benchmark circuits we simulated include *c17* and *c432* from ISCAS '85, *b02* from ITC '99, *s27* from ISCAS '89, carry generator for the third bit of a carry look-ahead adder (*cla*), and a 4-bit full adder (*4bit_fa*). Sequential circuits *b02* and *s27* are converted into combinational circuits by the pseudo prime input method in order to have a consistent datapath delay definition compatible with other circuits. The summary of these circuits are presented in Table III. We report delay, dynamic power, leakage power, total power, and EDP from circuits implemented in the four setups in Figure 20.

TABLE III
BENCHMARK CIRCUITS

Circuit	# of Gates	# of PI	# of PO
c17	6	5	2
b02	25	3	1
s27	10	4	1
cla	5	7	1
4bit_fa	20	9	5
c432	153	36	7

Summary of numbers of gates, primary inputs (PI), and primary outputs (PO) of the benchmark circuits used in our experiments.

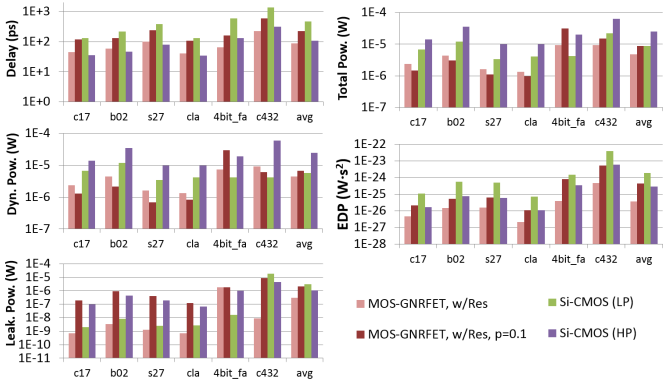


Fig. 20. Simulation of benchmark circuits, reporting delay, dynamic power, leakage power, total power, and EDP.

Based on results in Figures 19 and 20, line edge roughness plays a significant role in degrading the current in MOS-GNRFETs. As a result, Si-CMOS (HP) performs better in delay unless the MOS-GNRFET is ideal. In terms of dynamic power, MOS-GNRFET has lower consumption than Si-CMOS (HP) mostly due to lower V_{DD} and lower gate capacitance, and has comparable consumption to Si-CMOS (LP). In terms of leakage power for MOS-GNRFET, when a sufficiently high V_{DS} is applied, the confined states in the valence band of the channel align with the occupied states of the drain, resulting in band-to-band injection of holes in the channel [13]. This is captured in equation (15), which describes an exponential relation between V_{DD} and the tunneling probability. First of all, when $V_{DD} = 0.7$ V, MOS-GNRFET has a higher leakage power than Si-CMOS (HP) shown in Figure 15. However, when V_{DD} is smaller (e.g., 0.5 V), the tunneling is significantly reduced, consuming much lower leakage especially for the ideal case. Overall, ideal MOS-GNRFET has lower power consumption and comparable delay compared to Si-CMOS (HP), and it has lower delay and comparable power consumption compared to Si-CMOS (LP).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

In other words, ideal MOS-GNRFETs has advantages over both types of Si-CMOS transistors. However, MOS-GNRFET with nonidealities loses these benefits. In terms of EDP, ideal MOS-GNRFET performs the best, while MOS-GNRFET with $p_r = 10\%$ still has comparable EDP with Si-CMOS (HP).

In Figure 21, we compared the waveforms of two 11-stage ring oscillators, implemented with Si-CMOS (HP) and ideal MOS-GNRFET, respectively. Ideal MOS-GNRFET demonstrated a 5.5% higher frequency than Si-CMOS (HP), consistent with our observation in other circuits.

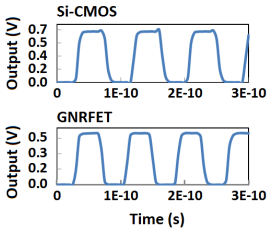


Fig. 21. Simulation of ring oscillators in Si-CMOS and ideal MOS-GNRFET.

5) Discussion on Running Time: We performed the SPICE simulations on a machine with a 1.4 GHz AMD Opteron CPU. A typical transient analysis of a MOS-GNRFET inverter took 2.56 seconds, *c17* took 27613.54 seconds ($\sim$ 7.67 hours), and *c432* took 30706.04 seconds($\sim$ 8.53 hours). In comparison, *c432* implemented with the PTM Si-CMOS model took only 22.98 seconds. The slowdown mainly comes from the subcircuit implementation of our MOS-GNRFET model, especially with the solver side-circuit construct (Figure 4 (b)) to solve for the non-closed-form V_{CH}, as compared to the PTM models' utilization of SPICE's default transistor implementation. Still, the NEGF transistor simulation done by ViDES or similar tools takes hours to simulate one DC analysis of a single transistor, and our SPICE model greatly improves the running time such that one DC analysis finishes within a second, so we can scale up to circuit-level simulations with some loss of accuracy as indicated by the mismatch between our model and the ViDES simulations, shown in Figures 8-12.

D. Monte Carlo Simulation of Process Variation

To evaluate the impact of process variation on the circuit level, Monte Carlo (MC) simulations are necessary. When we evaluated the effects of varied design parameters in the previous sections, only one parameter was varied at a given time, which does not reflect the reality where more than one parameter may vary from the nominal value. Also, the sensitivity of each parameter to the resulting delay and power can be studied using MC simulations. HSPICE-based Monte Carlo simulations were run on the *c17* benchmark of ISCAS'85 for ideal MOS-GNRFET with contact resistance, MOS-GNRFET with contact resistance and $p_r = 0.1$, and 16-nm Si-CMOS (HP) from PTM.

A global distribution was defined for modeling the systematic gate-to-gate variation in parameters and a local distribution was used to model the random intra-gate variation among transistors [37]. The values and the distribution for each parameter are shown in Table IV for Si-CMOS (HP) and in Table V for MOS-GNRFET, which are based on the assumptions made in [1], [38]. Note that for N, the numbers are rounded to integers.

TABLE IV
MONTE CARLO DISTRIBUTION PARAMETERS FOR SI-CMOS

Parameter	Distribution	Mean	Standard Deviation
Doping Level	Gaussian	2×10^{20}	2×10^{19}
Oxide Thickness T_{ox}	Gaussian	0.95 nm	0.1 nm
Channel Width W_{CH}	Gaussian	32 nm	3.2 nm

TABLE V
MONTE CARLO DISTRIBUTION PARAMETERS FOR MOS-GNRFET

Parameter	Distribution	Mean	Standard Deviation
Doping Level	Gaussian	2×10^{20}	2×10^{19}
Oxide Thickness T_{ox}	Gaussian	0.95 nm	0.1 nm
GNR Width N	Gaussian	12	1.2

1) Experiment Setup: Two random variables X and Y are independent if $P(X \wedge Y) = P(X)P(Y)$. The covariance between random variables X and Y is $COV(X,Y) = E[X - EX]E[Y - EY] = E[XY] - EXEY$. If $COV(X,Y) = 0$, X and Y are *uncorrelated*. If X and Y are independent then they are uncorrelated, but the converse is not true.

We utilize SPICE's built-in Monte Carlo feature in this set of experiments. All the design parameters used in the Monte Carlo simulations are generated as follows. Take one parameter, T_{ox} as an example. We first determine the average T_{ox} of each logic gate from a normal distribution (global distribution). Then, each transistor's actual T_{ox} is computed from the average T_{ox} of the gate added by a small amount of intra-gate variation, also from a normal distribution (local distribution). In our experiments and the example below, the local distribution's standard deviation is 0.1 of the global one. This is based on the fact that transistors within a logic gate are usually placed close to each other. Therefore, their design parameters should be highly correlated. This is to model intra-gate correlation in circuits despite the lack of actual placement information in HSPICE circuit implementation. Meanwhile, transistors not in the same logic gate have uncorrelated parameters. Despite not having placement information, a measurement study shows that within-die spatial correlation is almost nonexistent [39], and another study shows that a model with spatial correlation only has marginal effect on circuit optimization results over the model without [40].

We use a circuit that contain two *inv* gates, *inv_a* and *inv_b*, as shown in Figure 22, to demonstrate the computation of randomized design parameters. The inverters *inv_a* and *inv_b* are located far from each other in the circuit. Let X_A and X_B be random variables representing the average values of the design parameter in concern within *inv_a* and *inv_b*, respectively. Assume that the design parameter of each gate independently follows a normal distribution with mean μ and standard deviation σ under process variation. We have $X_A \sim N(\mu, \sigma)$ and $X_B \sim N(\mu, \sigma)$. Since X_A and X_B are independent and identically distributed (i.i.d.), $COV(X_A, X_B) = 0$, and their covariance matrix is simply

$$\begin{bmatrix} VAR(X_A) & COV(X_A, X_B) \\ COV(X_B, X_A) & VAR(X_B) \end{bmatrix} = \begin{bmatrix} \sigma^2 & 0 \\ 0 & \sigma^2 \end{bmatrix} \quad (27)$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

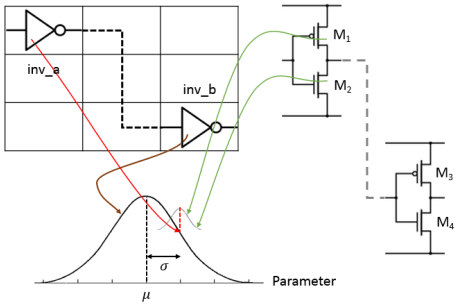


Fig. 22. Example illustrating the setup of Monte Carlo simulation. The transistor parameters in *inv_a* and *inv_b* come from the same global distribution (indicated by the large normal distribution). Within a gate, e.g. *inv_a*, each transistor has an additional local variation (indicated by the small normal distribution) superimposed on the global distribution.

Next, we add a small amount of intra-gate variation to each transistor. Let X_i be a random variable representing the design parameter value of transistor M_i. Let $\delta_i \sim N(0, 0.1\sigma)$ be a random variable representing the amount of intra-gate variation. We have

$$X_1 = X_A + \delta_1$$
$$X_2 = X_A + \delta_2$$
$$X_3 = X_B + \delta_3$$
$$X_4 = X_B + \delta_4$$

The covariance between X_1 and X_2 is

$$\begin{aligned} COV(X_1, X_2) &= E[X_1 - EX_1]E[X_2 - EX_2] \\ &= E[X_1X_2] - EX_1EX_2 \end{aligned}$$

where

$$\begin{aligned} E[X_1X_2] &= E[(X_A + \delta_1)(X_A + \delta_2)] \\ &= E[X_A^2] + E[X_A\delta_1] + E[X_A\delta_2] + E[\delta_1\delta_2] \\ &= (Var(X_A) + E^2[X_A]) + 0 + 0 + 0 \\ &= \sigma^2 + \mu^2 \end{aligned}$$

and thus

$$\begin{aligned} COV(X_1, X_2) &= (\sigma^2 + \mu^2) - \mu^2 \\ &= \sigma^2 \end{aligned}$$

meaning they are correlated. Meanwhile, the covariance between X_1 and X_3 is

$$\begin{aligned} COV(X_1, X_3) &= E[X_1 - EX_1]E[X_3 - EX_3] \\ &= E[X_1X_3] - EX_1EX_3 \end{aligned}$$

Since $E[X_AX_B] = E[X_A]E[X_B]$ as X_A and X_B are independent, we have

$$\begin{aligned} E[X_1X_3] &= E[(X_A + \delta_1)(X_B + \delta_3)] \\ &= E[X_AX_B] + E[X_A\delta_3] + E[X_B\delta_1] + E[\delta_1\delta_3] \\ &= E[X_A]E[X_B] + 0 + 0 + 0 \\ &= \mu^2 \end{aligned}$$

and thus

$$\begin{aligned} COV(X_1, X_3) &= \mu^2 - \mu^2 \\ &= 0 \end{aligned}$$

meaning they are uncorrelated. Therefore, the covariance matrix of X_1, X_2, X_3, and X_4 is

$$\begin{bmatrix} VAR(X_1) & COV(X_1,X_2) & COV(X_1,X_3) & COV(X_1,X_4) \\ COV(X_2,X_1) & VAR(X_2) & COV(X_2,X_3) & COV(X_2,X_4) \\ COV(X_3,X_1) & COV(X_3,X_2) & VAR(X_3) & COV(X_3,X_4) \\ COV(X_4,X_1) & COV(X_4,X_2) & COV(X_4,X_3) & VAR(X_4) \end{bmatrix}$$
$$= \begin{bmatrix} \sigma^2 & \sigma^2 & 0 & 0 \\ \sigma^2 & \sigma^2 & 0 & 0 \\ 0 & 0 & \sigma^2 & \sigma^2 \\ 0 & 0 & \sigma^2 & \sigma^2 \end{bmatrix}$$

In this example, we show that our randomization method results in positively correlated transistors in the same logic gate, while the transistors in different logic gates are uncorrelated.

2) Simulation Results: The High-Performance (HP) 16-nm Si-CMOS serves as a baseline for the subsequent simulations of MOS-GNRFET circuits. The *c17* simulation results for Si-CMOS when all parameters are varied are given in Figure 23. The results for ideal MOS-GNRFET are given in Figure 24. The results for MOS-GNRFET with contact resistance and $p_r = 0.1$ are given in Figure 25.

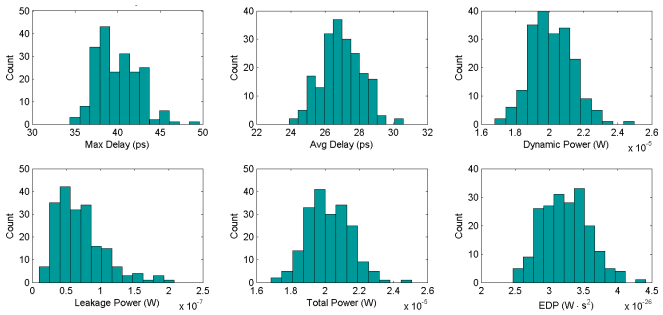


Fig. 23. Monte Carlo simulation of a Si-CMOS *c17* circuit with all three parameters varied.

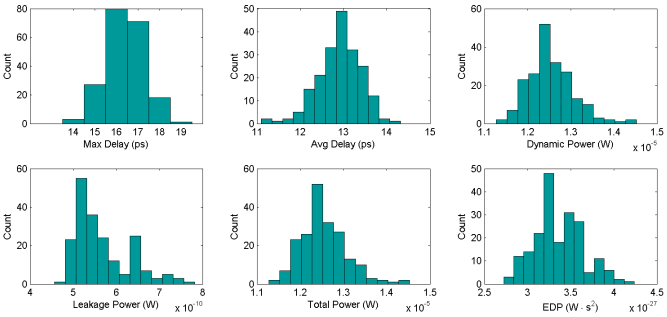


Fig. 24. Monte Carlo simulation of a *c17* circuit of ideal MOS-GNRFET with contact resistance with all three parameters varied.

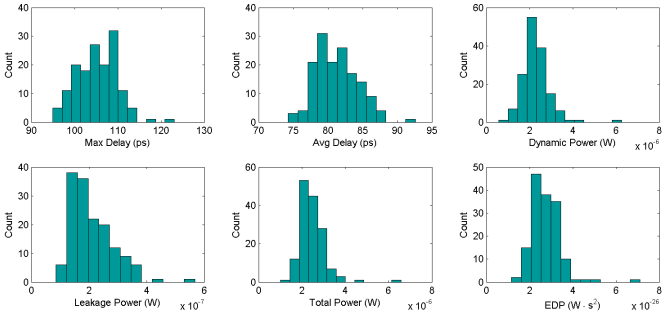


Fig. 25. Monte Carlo simulation of a *c17* circuit of MOS-GNRFET with contact resistance and $p_r = 0.1$ with all three parameters varied.

3) Discussion: We analyze the Monte Carlo simulation results based on the exploration in Section IV-C3. For N variation, I_{on} and I_{off} both change drastically, as shown in Figure 9. Figure 18 shows that f_{dop} changes the I_{on} and I_{off} more than T_{ox} and L_{CH}, and thus it is the dominating factor when

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

these parameters are varied simultaneously. For f_{dop}, I_{on} only changes when the f_{dop} varies for a few orders of magnitude, but I_{off} decreases exponentially with f_{dop} when doping is low, as shown in Figure 10. For T_{ox} variation, I_{on} increases exponentially with T_{ox} and I_{off} decreases exponentially with T_{ox}, but not as drastically as with f_{dop} variation. L_{CH} only has a second-order effect on I_{on} and I_{off}.

As I_{on} and I_{off} is dominated by f_{dop}, the leakage power follows a log-normal distribution, as I_{off} has an exponential relationship with doping. Delay, dynamic power, and total power follow a bell-shaped distribution skewed to the left as I_{on} is linear in f_{dop} but is exponential in T_{ox}, thus making the distribution a mixture of normal and log-normal. EDP is computed from delay and total power and follows a distribution that is close to normal. For channel width variation, the effect on Si-CMOS is continuous, whereas for MOS-GNRFET, the GNR width is discrete, and therefore the effects are more discrete. Note that for MOS-GNRFET circuits, there are a few outliers that fall outside of the normal or log-normal distribution. This is likely because a different value of N was chosen for a transistor and caused it to have a very different I-V curve.

In the above simulations, only a relatively simple circuit was simulated due to the time-consuming nature of Monte Carlo simulations. As discussed in Section IV-C5, each data point of one transient analysis of *c17* takes up to hours to complete. We also did not consider spatial correlation due to the lack of layout information in SPICE-level netlists, only intra-gate correlation. Evaluation on large-scale circuits with more elaborate variation modeling such as spatial correlation would require a different framework, such as integration with higher-level CAD tools.

V. Conclusion and Future Work

We presented a parameterized, SPICE-compatible compact model of a MOS-type GNRFET. It captured the effects of V_{DD}, $N(W_{CH})$, L_{CH}, T_{ox}, f_{dop}, and line edge roughness on current and charge. In addition, we presented a GNR-based circuit architecture that integrates gates and interconnects. The model and the architecture allow circuit-level performance evaluations of GNRFETs under process variation. We observed that GNRFETs are promising compared to Si-CMOS since they have either lower delay or lower power. We also showed that ribbon width variation and line edge roughness can critically reduce the performance and leakage power advantages of GNRFETs, which is a major shortcoming of this emerging technology.

In terms of process variation evaluation, we performed a series of deterministic and Monte Carlo simulations to show the effects from each design parameter and provided various insights on the different aspects of GNRFET's performances. Such data may provide early guidance for future experimental studies of GNRFETs.

A SPICE implementation of the presented model has been released at https://nanohub.org/resources/17074.

Acknowledgment

This work is partially supported by NSF under the grant CCF 07-46608.

References

[1] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstrom, and H. Dai, "Carbon nanotube field-effect transistors with integrated ohmic contacts and high-k gate dielectrics," *Nano Letters*, vol. 4, no. 3, pp. 447–450, 2004.

[2] S. Chilstedt, C. Dong, and D. Chen, "Carbon nanomaterials transistors and circuits, transistors: Types, materials and applications," *Nova Science Publishers*, 2010.

[3] W. de Heer, C. Berger, E. Conrad, P. First, R. Murali, and J. MeindI, "Pionics: the emerging science and technology of graphene-based nanoelectronics," in *Electron Devices Meeting (IEDM), IEEE International*, 2007, pp. 199 –202.

[4] M. P. Levendorf, C. S. Ruiz-Vargas, S. Garg, and J. Park, "Transfer-free batch fabrication of single layer graphene transistors," *Nano Letters*, vol. 9, no. 12, pp. 4479–4483, 2009.

[5] P. J. Wessely, F. Wessely, E. Birinci, U. Schwalke, and B. Riedinger, "Transfer-free fabrication of graphene transistors," *Journal of Vacuum Science and Technology B*, vol. 30, no. 3, 2012.

[6] A. Betti, G. Fiori, and G. Iannaccone, "Strong mobility degradation in ideal graphene nanoribbons due to phonon scattering," *Applied Physics Letters*, vol. 98, no. 21, p. 212111, 2011.

[7] Y.-W. Son, M. L. Cohen, and S. G. Louie, "Energy gaps in graphene nanoribbons," *Phys. Rev. Lett.*, vol. 97, p. 216803, 2006.

[8] K. Nakada and M. Fujita, "Edge state in graphene ribbons: Nanometer size effect and edge shape dependence," *Phys. Rev. B, Condense Matter*, vol. 54, pp. 17 954–17 961, 1996.

[9] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors," *Phys. Rev. Lett.*, vol. 100, p. 206803, May 2008.

[10] H. Raza, "Zigzag graphene nanoribbons: bandgap and midgap state modulation," *Journal of Physics: Condensed Matter*, vol. 23, no. 38, p. 382203, 2011.

[11] G. Fiori and G. Iannaccone, "Simulation of graphene nanoribbon field-effect transistors," *Elec. Dev. Lett.*, vol. 28, no. 8, pp. 760 –762, 2007.

[12] Y. Yoon, G. Fiori, S. Hong, G. Iannaccone, and J. Guo, "Performance comparison of Graphene Nanoribbon FETs with Schottky contacts and doped reservoirs," *Electron Devices, IEEE Transactions on*, vol. 55, no. 9, pp. 2314 –2323, 2008.

[13] P. Michetti and G. Iannaccone, "Analytical model of one-dimensional carbon-based Schottky-barrier transistors," *Electron Devices, IEEE Transactions on*, vol. 57, no. 7, pp. 1616 –1625, 2010.

[14] M. Choudhury, Y. Yoon, J. Guo, and K. Mohanram, "Technology exploration for graphene nanoribbon FETs," in *IEEE/ACM Design Automation Conference*, 2008, pp. 272 –277.

[15] S. Fregonese, C. Maneux, and T. Zimmer, "A versatile compact model for ballistic 1D transistor: Applications to GNRFET and CNTFET," in *International Semiconductor Device Research Symposium*, 2009, pp. 1 –2.

[16] J. Deng and H.-S. Wong, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application part I: Model of the intrinsic channel region," *Electron Devices, IEEE Transactions on*, vol. 54, no. 12, pp. 3186 –3194, 2007.

[17] ——, "A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application part II: Full device model and circuit performance benchmarking," *Electron Devices, IEEE Transactions on*, vol. 54, no. 12, pp. 3195 –3205, 2007.

[18] M. B. Henry and S. Das, "SPICE-compatible compact model for graphene field-effect transistors," in *International Symposium on Circuits and Systems*, 2012, pp. 2521 –2524.

[19] "NanoHub," http://www.nanohub.org, 2013.

[20] T. Yan, Q. Ma, S. Chilstedt, M. D. F. Wong, and D. Chen, "A routing algorithm for graphene nanoribbon circuit," *ACM Transactions on Design Automation of Electronic Systems*, vol. 18, no. 4, pp. 61:1–61:18, Oct. 2013. [Online]. Available: http://doi.acm.org/10.1145/2505056

[21] S. S. Chauhan, P. Srivastava, and A. K. Shrivastava, "Band gap engineering in zigzag graphene nanoribbons an *Ab Initio* approach," *Journal of Computational and Theoretical Nanoscience*, vol. 9, no. 8, pp. 1084–1089, 2012-08-01T00:00:00.

[22] "Nano TCAD ViDES," http://vides.nanotcad.com/vides/, 2011.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNANO.2015.2469647, IEEE Transactions on Nanotechnology

[23] Z. Chen, Y.-M. Lin, M. J. Rooks, and P. Avouris, "Graphene nano-ribbon electronics," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 40, no. 2, pp. 228 – 232, 2007.

[24] X. Wang and H. Dai, "Etching and narrowing of graphene from the edges," *Nature Chemistry*, vol. 2, pp. 661–665, 2010.

[25] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, "Chemically derived, ultrasmooth graphene nanoribbon semiconductors," *Science*, vol. 319, no. 5867, pp. 1229–1232, 2008.

[26] J. Cai, P. Ruffieux, R. Jaafar, M. Bieri, T. Braun, S. Blankenburg, M. Muoth, A. P. Seitsonen, M. Saleh, X. Feng, K. Mllen, and R. Fasel, "Atomically precise bottom-up fabrication of graphene nanoribbons," *Nature*, vol. 466, pp. 470–473, July 2010.

[27] L. Jiao, L. Zhang, L. Ding, J. Liu, and H. Dai, "Aligned graphene nanoribbons and crossbars from unzipped carbon nanotubes," *Nano Research*, vol. 3, no. 6, pp. 387–394, 2010. [Online]. Available: http://dx.doi.org/10.1007/s12274-010-1043-z

[28] S. Prezioso, F. Perrozzi, M. Donarelli, F. Bisti, S. Santucci, L. Palladino, M. Nardone, E. Treossi, V. Palermo, and L. Ottaviano, "Large area extreme-UV lithography of graphene oxide via spatially resolved photoreduction," *Langmuir*, vol. 28, no. 12, pp. 5489–5495, 2012.

[29] K. Nagashio, T. Nishimura, K. Kita, and A. Toriumi, "Metal/graphene contact as a performance killer of ultra-high mobility graphene analysis of intrinsic mobility and contact resistance," in *Electron Devices Meeting (IEDM), IEEE International*, 2009, pp. 1 –4.

[30] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge University Press, 2010.

[31] S. Mukhopadhyay, A. Raychowdhury, and K. Roy, "Accurate estimation of total leakage in nanometer-scale bulk cmos circuits based on device geometry and doping profile," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 24, no. 3, pp. 363–381, March 2005.

[32] S. Fregonese, C. Maneux, and T. Zimmer, "Implementation of tunneling phenomena in a cntfet compact model," *Electron Devices, IEEE Transactions on*, vol. 56, no. 10, pp. 2224–2231, Oct 2009.

[33] "FastCap 2," http://www.fastfieldsolvers.com, 2013.

[34] G. H. See, X. Zhou, K. Chandrasekaran, S. B. Chiah, Z. Zhu, C. Wei, S. Lin, G. Zhu, and G. H. Lim, "A compact model satisfying gummel symmetry in higher order derivatives and applicable to asymmetric mosfets," *Electron Devices, IEEE Transactions on*, vol. 55, no. 2, pp. 624–631, Feb 2008.

[35] I. Hajj, "On device modeling for circuit simulation with application to carbon-nanotube and graphene nano-ribbon field-effect transistors," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, no. 99, pp. 495–499, Jan 2015.

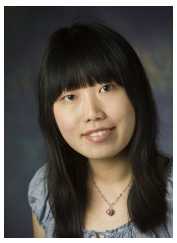
[36] "Predictive technology model," http://www.ptm.asu.edu, 2013.

[37] C. C. McAndrew, "Statistical modeling for circuit simulation," in *Proc. IEEE International Symposium on Quality Electronic Design*, 2003, pp. 357–362.

[38] J. Zhang, N. Patil, A. Hazeghi, H. S. P. Wong, and S. Mitra, "Characterization and design of logic circuits in the presence of carbon nanotube density variations," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 30, no. 8, pp. 1103–1113, Aug 2011.

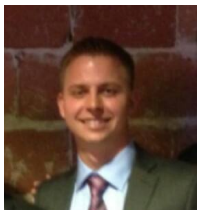
[39] N. Drego, A. Chandrakasan, and D. Boning, "An all-digital, highly scalable architecture for measurement of spatial variation in digital circuits," in *Solid-State Circuits Conference, 2008. A-SSCC '08. IEEE Asian*, Nov 2008, pp. 393–396.

[40] Q. Y. Tang, P. Friedberg, G. Cheng, and C. Spanos, "Circuit size optimization with multiple sources of variation and position dependant correlation," vol. 6521, March 2007, pp. 1–11.



Ying-Yu (Christine) Chen received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2008. She is currently pursuing the M.S./Ph.D. degrees in electrical and computer engineering with the University of Illinois at Urbana-Champaign, Champaign, IL, USA. She interned at Intels Strategic CAD Labs, Hillsboro, OR, USA, in 2011.

Amit Sangai Amit Sangai received the B.S. and M.S. in electrical engineering at the University of Illinois at Urbana-Champaign, Champaign, IL, USA. His research focused on GNRFET circuit simulation.



Artem Rogachev received the M.S. degree in electrical and computer engineering from University of Illinois at Urbana Champaign in 2012. His master's research focused on modeling graphene-based transistor and statistical static timing analysis. Currently, he works as a systems engineer for Texas Instruments.

Morteza Gholipour (S01-M15) received the Ph.D. degree in electrical and electronic engineering from the University of Tehran, Tehran, Iran, in 2014. He was a Visiting Scholar with the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 2013. He is currently with the Babol University of Technology, Babol, Iran. His current research interests include nanoelectronic circuits design, and GNR and CNT device modeling and simulation.

Giuseppe Iannaccone (M98SM10-F15) is professor of electronics at University of Pisa, Italy.His research interests include nanoelectronics and quantum transport, design of nanopower analog integrated circuits, RFID and smart systems. He has published more than 170 papers in peer-reviewed journals and more than 120 papers in proceedings of international conferences. Visit him at www.iannaccone.org or on @iannak1.

Gianluca Fiori is an Assistant Professor with the University of Pisa, Pisa, Italy. He is the leading developer of the open-source code NanoTCAD ViDES. His current research interests include the simulation of 2-D material based transistors and the performance assessment of novel nanoscale devices.

Deming Chen obtained his BS in computer science from University of Pittsburgh, PA in 1995, and his MS and PhD in computer science from University of California at Los Angeles in 2001 and 2005 respectively. He is a professor in the ECE department of University of Illinois, Urbana-Champaign. His current research interests include system-level and high-level synthesis, nano-systems design and nano-centric CAD techniques, GPU and reconfigurable computing, hardware security, and computational genomics. Dr. Chen is a technical committee member of FPGA, ASPDAC, ICCD, ISQED, DAC, ICCAD, DATE, ISLPED, FPL, etc. He is the General Chair for SLIP'12, the CANDE Workshop Chair in 2011, the Program Chair for PROFIT'12, and Program Chair for FPGA'15. He is or has been an associated editor for TCAD, TODAES, TVLSI, TCAS-I, JCSC, and JOLPE. He obtained the Achievement Award for Excellent Teamwork from Aplus Design Technologies in 2001, the Arnold O. Beckman Research Award from UIUC in 2007, the NSF CAREER Award in 2008, and five Best Paper Awards for ASPDAC'09, SASP'09, FCCM'11, SAAHPC'11, and CODES+ISSS'13. He is included in the List of Teachers Ranked as Excellent in 2008. He received the ACM SIGDA Outstanding New Faculty Award in 2010, and IBM Faculty Award in 2014 and 2015. He is a senior member of IEEE and the Donald Biggar Willett Faculty Scholar.