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A first-principles study on the effect of biaxial strain on the ultimate performance of monolayer MoS2-based double gate field effect transistor
Comparison of short-channel effects in monolayer MoS$_2$ based junctionless and inversion-mode field-effect transistors

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Conventional junctionless (JL) multi-gate (MuG) field-effect transistors (FETs) require extremely scaled channels to deliver high on-state current with low short-channel effect related leakage. In this letter, using ultra-thin 2D materials (e.g., monolayer MoS$_2$), we present comparison of short-channel effects in JL, and inversion-mode (IM) FETs. We show that JL FETs exhibit better sub-threshold slope (S.S.) and drain-induced-barrier-lowering (DIBL) in comparison to IM FETs due to reduced peak electric field at the junctions. But, threshold voltage ($V_T$) roll-off with channel length downscaling is found to be significantly higher in JL FETs than IM FETs, due to higher source/drain controlled charges ($dE/dx$) in the channel. Further, we show that although $V_T$ roll-off in JL FETs improves by increasing the gate control, i.e., by scaling the oxide, or channel thickness, the sensitivity of threshold voltage on structural parameters is found out to be high.

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Novel materials and device structures have been explored in order to continue scaling of MOSFET devices. Multi-gate (MuG) field-effect transistors (FETs), due to their excellent gate control, are being pursued for current, and upcoming technology nodes. Moreover, junctionless (JL) MuGFET has been proposed as a potential future device option showing better scalability, and fabrication simplicity in comparison to inversion-mode (IM) FETs. Due to its operation based on pinch-off of the channel by means of depletion, JL FETs require extremely scaled channels, or body in order to achieve better gate control, and low leakage.1,2

Recently, the emergence of a class of 2D semiconducting materials such as transition metal dichalcogenides (TMDs) have enabled the possibility of atomic thin channels in FETs for better gate control. For example, monolayer MoS$_2$ FET has been shown to have better scalability than an ultra-thin-body (UTB) Si FET due to monolayer thin body, and higher effective mass, resulting in reduced direct source-to-drain tunneling.3 Moreover, a sub-threshold slope (S.S.) of 60 mV/dec has been demonstrated in monolayer WSe$_2$ FET.4

In this letter, we present a study discussing channel length scaling of monolayer MoS$_2$ based junctionless and inversion-mode FETs. Using atomistic two-band ballistic quantum transport simulations, we show that JL FETs promise better scalability than IM FETs considering short-channel effects (SCEs) such as S.S. and drain-induced-barrier-lowering (DIBL). But, surprisingly JL FETs show worse threshold voltage ($V_T$) control with channel length downscaling in comparison to IM FETs, resulting in higher $V_T$ roll-off. We further discuss the underlying mechanism for such improvement in S.S. and DIBL, and reduction of threshold voltage with channel length downscaling. It is explained that although JL FETs manifest reduced electric field at the junctions in comparison to IM FETs, JL FETs also show higher gradient of lateral electric field in channel, i.e., higher source/drain controlled charges ($dE/dx$) in the channel. We further show that we require better gate control in JL FETs than IM FETs for lower $V_T$ roll-off, which can be achieved by further scaling the oxide thickness or the channel thickness.

Monolayer MoS$_2$ based IM and JL FETs in double-gate configuration are schematically shown in Fig. 1. It is important to note here that we use abrupt source/drain junctions, and no gate overlap in IM FETs to compare both non-optimized IM and JL FETs with same structural parameters such as oxide thickness ($t_{HfO_2}$) and channel length ($L_{CH}$). Moreover, we use

![FIG. 1. Schematic of monolayer MoS$_2$ based (a) inversion-mode FET and (b) junctionless FET in double-gate configuration with $L_S=L_D=15$nm, $n^+$ doping of $1.5 \times 10^{13}$ cm$^{-2}$, $t_{HfO_2} = 4.9$nm with $t_{HfO_2} = 25$, $t_{CH} = 0.7$nm, and $L_{CH} = 6-30$nm.](Image)

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same doping concentration of $1.5 \times 10^{13} \text{ cm}^{-2}$ for $n^+$ doping in JL FETs, and source/drain regions for IM FETs using similar chemical doping techniques as demonstrated in Ref. 4, while the MoS$_2$ channel in IM FET is assumed to be intrinsically $n^-$ doped from the environment, as reported in experimental works such as in Ref. 5. The electrical characteristics of both IM and JL FETs are simulated using two-band tight binding (TB) Hamiltonian with an open source quantum transport simulation framework based on self-consistent solution of Poisson and Schrödinger equation in non-equilibrium Green’s function framework. Further, the two-band Hamiltonian can be defined as a $2 \times 2$ Hamiltonian matrix, which is based on a unit cell of two-dissimilar atoms such M and X in MX$_2$ materials, and can be written as

$$H_{CH} = \begin{bmatrix} E_C & tf(k) \\ tf^*(k) & E_V \end{bmatrix},$$  

where $E_C$ and $E_V$ represent bottom of conduction band and the top of the valence band, which is related to bandgap ($E_G$) of the material as: $E_G = E_C - E_V$. While $t$ represents in-plane hopping energy which is fitted for a specified effective mass ($m^*$), and $f(k)$ function, due to nearest neighbors, can be written as

$$f(k) = e^{ik_x a/\sqrt{3}} + 2e^{-ik_x a/2\sqrt{3}} \cos \left( \frac{k_y a}{2} \right).$$  

Here, $k_x$ and $k_y$ are wave vectors in x and y directions of our device, while $a$ represents distance between M and X atoms. Further, using secular equation, we obtain dispersion relation for two-band model given as

$$E^\pm(k) = \frac{(E_C + E_V) \pm \sqrt{(E_C - E_V)^2 + 4t^2|f(k)|^2}}{2},$$  

which provides a good approximation for lowest conduction band, and highest valence band of monolayer MX$_2$ materials for the considered bias ranges. For monolayer MX$_2$ materials, the two-band Hamiltonian parameters are calculated using the effective mass of conduction (n-FET) or valence band (p-FET), and bandgap of the material. Further, we extend the model for bilayer MX$_2$ materials using an inter-layer hopping parameter in the Hamiltonian, accounting for inter-layer coupling between the two layers. Here, monolayer MoS$_2$ channel is modeled with an electron effective mass of 0.45 $m_0$, and bandgap energy of 1.8 eV, while the bilayer MoS$_2$ channel is modeled with an electron effective mass of 0.62 $m_0$ and a bandgap of 1.3 eV.

With different gate work functions for IM ($\phi_M = 4.6 \text{ eV}$) and JL FETs ($\phi_M = 5.4 \text{ eV}$), the transfer characteristics of both FETs are shown in Fig. 2 with channel length scaling. We can observe that JL-FET with monolayer MoS$_2$ shows better electrostatic integrity with channel length ($L_{CH}$) downscaling. To have a closer look at SCE parameters, we plot S.S., DIBL, and $V_T$ roll-off extracted from transfer characteristics of IM and JL FETs, as shown in Fig. 3. Here, $V_T$ is extracted from transfer characteristics of both FETs using constant current method at a given normalized drain current ($I_D/W$) = $I_{ref}/L_{CH}$, where $W$ is the width of the channel, and $I_{ref}$ is chosen to be 250 nA. It can be seen from Fig. 3(a) that JL FET shows lower S.S. and DIBL with channel length downscaling in comparison to conventional inversion-mode FET, as reported in literature for multi-gate FETs. But, surprisingly JL FETs show worse threshold voltage ($V_T$) control with channel length scaling in comparison to IM FETs, as shown in Fig. 3(b).
To understand the underlying mechanism for such improvement in S.S. and DIBL, we plot the off-state conduction band energy minima ($E_C$) along the channel, showing the source-to-channel barrier in off-state ($V_T - V_{DD}/3$) which effectively determines the off-state current. Fig. 4(a) shows the off-state $E_C(x)$ along the channel at the middle of the width of monolayer MoS$_2$ channel. It can be observed from Fig. 4(a) that both height and width of source/channel barrier are larger for JL FETs in comparison to IM FETs. The larger width of the barrier prevents source-to-drain direct tunneling components, resulting in overall lesser leakage current. Further, as shown in Fig. 4(b), the absolute value of lateral electric field at source/channel, and channel/drain junctions are significantly lower in JL FETs in comparison to IM FETs, resulting in larger depletion lengths inside the drain extension, and thus lowering the effect of drain bias on source/channel barrier in JL FETs. Deep depletion inside source/drain extensions has been reported to result in improvement in S.S. and DIBL in JL FETs in comparison to IM FETs, which effectively results in larger width of the barrier and lower lateral electric fields at the junctions in JL FETs.$^{10,11}$

But, surprisingly JL FET exhibits larger $V_T$ roll-off in comparison to IM FET due to higher source/drain controlled charges inside channel at downscaled channel lengths. To understand it quantitatively, we can write charge density inside monolayer MoS$_2$ channel ($n_{2D}$) as

$$n_{2D} = n_G + n_{SD}. \tag{4}$$

Here, $n_G$ for a symmetrical double-gate FET is obtained as

$$n_G = 2C_G(V_{GS} - V_{FB} - \phi(x)). \tag{5}$$

where $C_G$, $V_{FB}$, and $\phi(x)$ represent the effective gate capacitance including quantum capacitance expressed in F/cm$^2$, flat-band voltage, and surface potential inside channel, respectively. While $n_{SD}$ can be written as

$$n_{SD} = \epsilon_{CH}qC_{CH} \left( \frac{dE}{dx} \right), \tag{6}$$

where $\epsilon_{CH}$ and $q$ represent dielectric constant of monolayer MoS$_2$ channel and electron charge, respectively. Eq. (6) establishes a direct relationship of source/drain controlled charges on gradient of lateral electric field. As shown in Fig. 4(c), $dE/dx$ inside the channel increases significantly in JL FETs with channel length scaling in comparison to IM FETs, resulting in larger $V_T$ roll-off in JL FETs.

From the discussion above, we show that S.S., DIBL, and $V_T$ roll-off for JL FETs need to be analyzed differently from IM FETs, as JL FETs operate on a principle of depleting the channel rather than inverting it. Therefore, for S.S. and DIBL, we look at the electrostatic potential/electric field profiles at the junctions and outside the channel, as the improvement in S.S. and DIBL for JL FETs arises due to deep depletion in source/drain regions, thus resulting in reduced electric field at the junctions, and direct source to drain tunneling. While for threshold voltage ($V_T$) roll-off, we calculate the charges present inside the channel, which consists of gate and source/drain controlled charges.

Further, we can write source/drain charges controlled component of threshold voltage ($V_T$) as

$$V_T = \lambda_{2D}^2 \frac{dE}{dx}, \tag{7}$$

where $\lambda_{2D}$ is the characteristic (scaling) length of symmetrical double-gate 2D material based FET, which can be written as$^{12}$
Thus, improving the gate control (i.e., lowering $\lambda_{2D}$) promises to improve $V_T$ control in JL FETs with channel length downscaling. Fig. 5 shows that although there is an improvement in $V_T$ roll-off by scaling the oxide or channel thickness, we observe that $V_T$ of JL FETs is highly sensitive to structural parameters such as oxide thickness and channel thickness. Moreover, it is important to note here that from electrostatic perspective JL FETs may perform inferior to IM FETs in case of thicker channels materials, due to increased equivalent-oxide-thickness in JL FETs.

In this letter, we present comparison of short-channel effects of monolayer MoS$_2$ based JL, and IM FETs. We show that although JL FET shows better electrostatic integrity from S.S. and DIBL point of view, it shows worse threshold voltage ($V_T$) control with channel length downscaling in comparison to IM FET. Further, due to larger $dE/dx$ in channel, an increased gate control by scaling the oxide thickness does not result in a significant improvement in $V_T$ roll-off of JL FETs. Poor threshold-voltage control in JL FETs may give rise to problems for circuit designers while using JL FETs in digital logic circuits, arising the need of adaptive biasing.

![Figure 5](image)

**FIG. 5.** Impact of scaling the oxide thickness and channel thickness on threshold voltage in JL FETs.

$$\lambda_{2D} = \frac{t_{HfO_2} + t_{CH} + t_{HfO_2}}{\pi}. \quad (8)$$